MAX5945xAX
Rev. A

RELIABILITY REPORT

FOR

MAX5945xAX

PLASTIC ENCAPSULATED HYBRID

April 4, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX5945 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5945 quad network power controller is designed for use in IEEE 802.3af-compliant power sourcing equipment (PSE). The device provides power devices (PD) discovery, classification, current limit, and both DC and AC load disconnect detections. The MAX5945 can be used in either endpoint PSE (LAN switches/routers) or midspan PSE (power injector) applications.

The MAX5945 can operate autonomously or be controlled by software through an I2C*-compatible interface. Separate input and output data lines (SDAIN and SDAOUT) allow usage with optocouplers. The MAX5945 is a slave device. Its four address inputs
allow 16 unique MAX5945 addresses. A separate INT output and four independent shutdown inputs (SHD_) allow fast response from a fault to port shutdown. A RESET input allows hardware reset of the device. A special Watchdog feature allows the hardware to gracefully take over control if the software crashes. A cadence timing feature allows the MAX5935 to be used
in midspan systems.

The MAX5945 is fully software configurable and programmable. A class-over-current detection function enables system power management to detect if a PD draws more current than the allowable amount for its class. Other features are input under/overvoltage lockout, overtemperature protection, output voltage slew-rate limit during startup, power-good, and fault status. The MAX5935's programmability includes gate charging current, currentlimit threshold, startup timeout, overcurrent timeout, autorestart duty cycle, PD disconnect AC detection threshold, and PD disconnect detection timeout.

The MAX5945 is available in a 36-pin SSOP package and is rated for both extended (-40°C to +85°C) and commercial (0°C to +70°C) temperature ranges.

B. Absolute Maximum Ratings

Item	Rating
(Voltages referenced to VEE, unless otherwise noted.)	
AGND, DGND, DET_, VDD, RESET, A3, A2, A1, A0, SHD_, OSC_IN, SCL, SDAIN, OUT_ and AUTO	-0.3V to +80V
GATE_ (Internally Clamped, Note 1)	-0.3V to +11.4V
SENSE_	-0.3V to +24V
VDD, RESET, A3, A2, A1, A0, SHD_, OSC_IN, SCL, SDAIN And AUTO to DGND	-0.3V to +7V
INT and SDAOUT to DGND	-0.3V to +12V
Maximum Current into INT, SDAOUT, DET_	80mA
Maximum Power Dissipation	
36-Pin SSOP (derate 11.4mW/°C above +70°C)	941mW
Operating Temperature Ranges:	
MAX5935EAX	-40°C to +85°C
MAX5935CAX	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Quad Network Power Controller for Power-Over-LAN
B. Process:	BCD80 & B6
C. Number of Device Transistors:	148,768
D. Fabrication Location:	Oregon and California, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	November, 2004

III. Packaging Information

A. Package Type:	**36-Pin SSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 31-4777
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	170 X 230 / 120 X 180
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn) / 0.6 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn) / 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{1000 \times 4340 \times 242 \times 2}$$

4.04 (Chi square value for MTTF upper limit)

1000 x 4340 x 242 x 2: Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 1.93 \times 10^{-9}$

λ = 1.93 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6162) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The NP50 die type has been found to have all pins able to withstand a transient pulse of <±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX5945xAX

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test					
	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality		242	1
Infant Mortality Test					
	Ta = 135°C Biased Time = 12 hrs.	DC Parameters & functionality		3080	0
Moisture Testing					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SSOP	236	0
HAST	Ta = 130°C RH = 85% Biased Time = 100hrs.	DC Parameters & functionality		139	0
Mechanical Stress					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		503	0

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

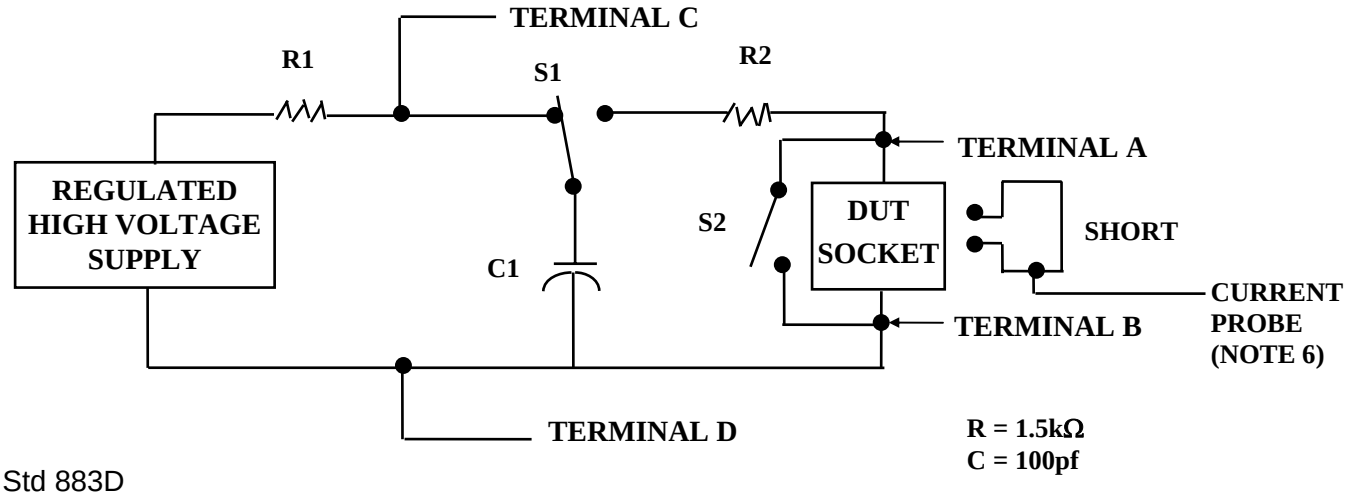
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

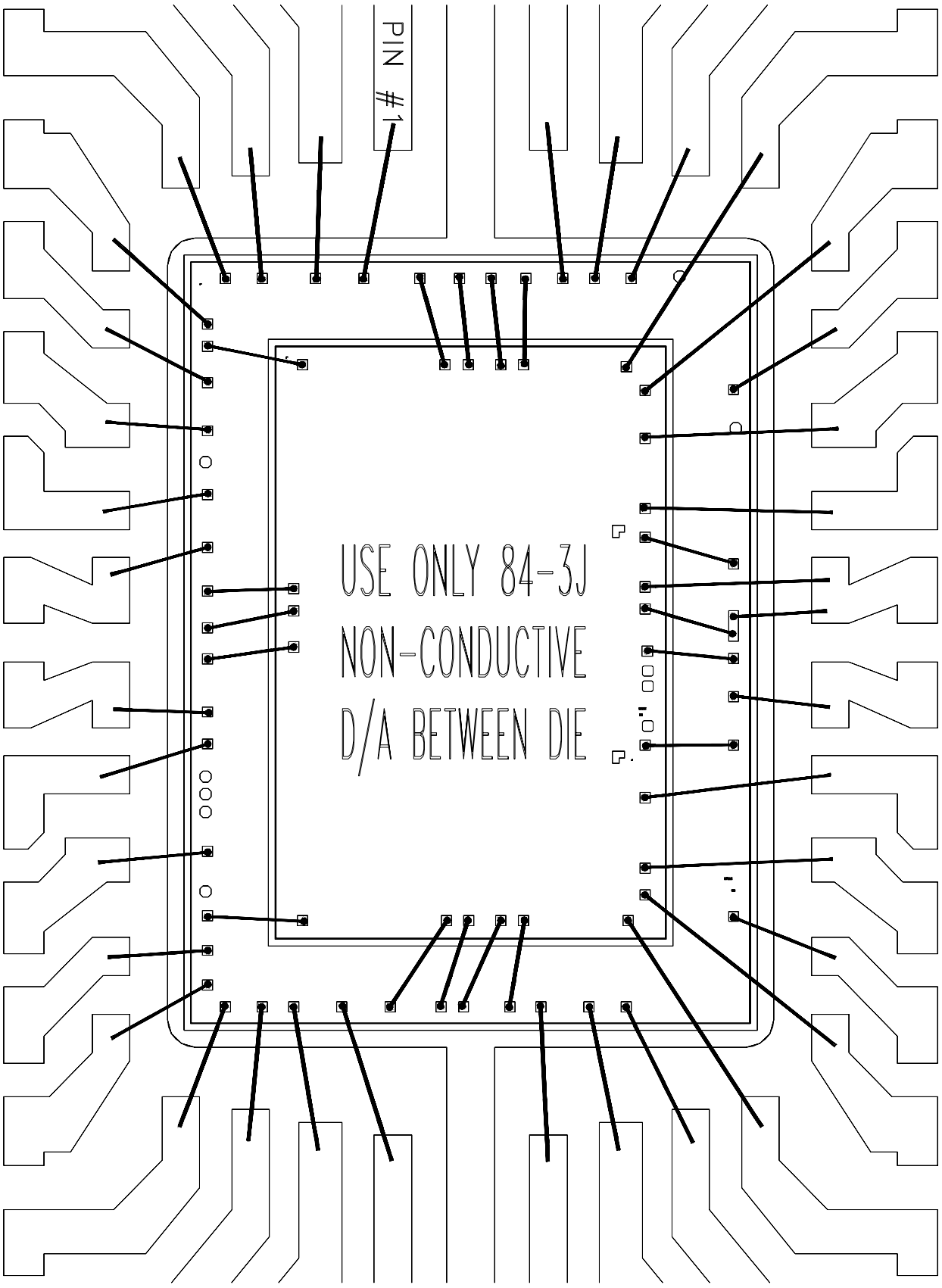
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





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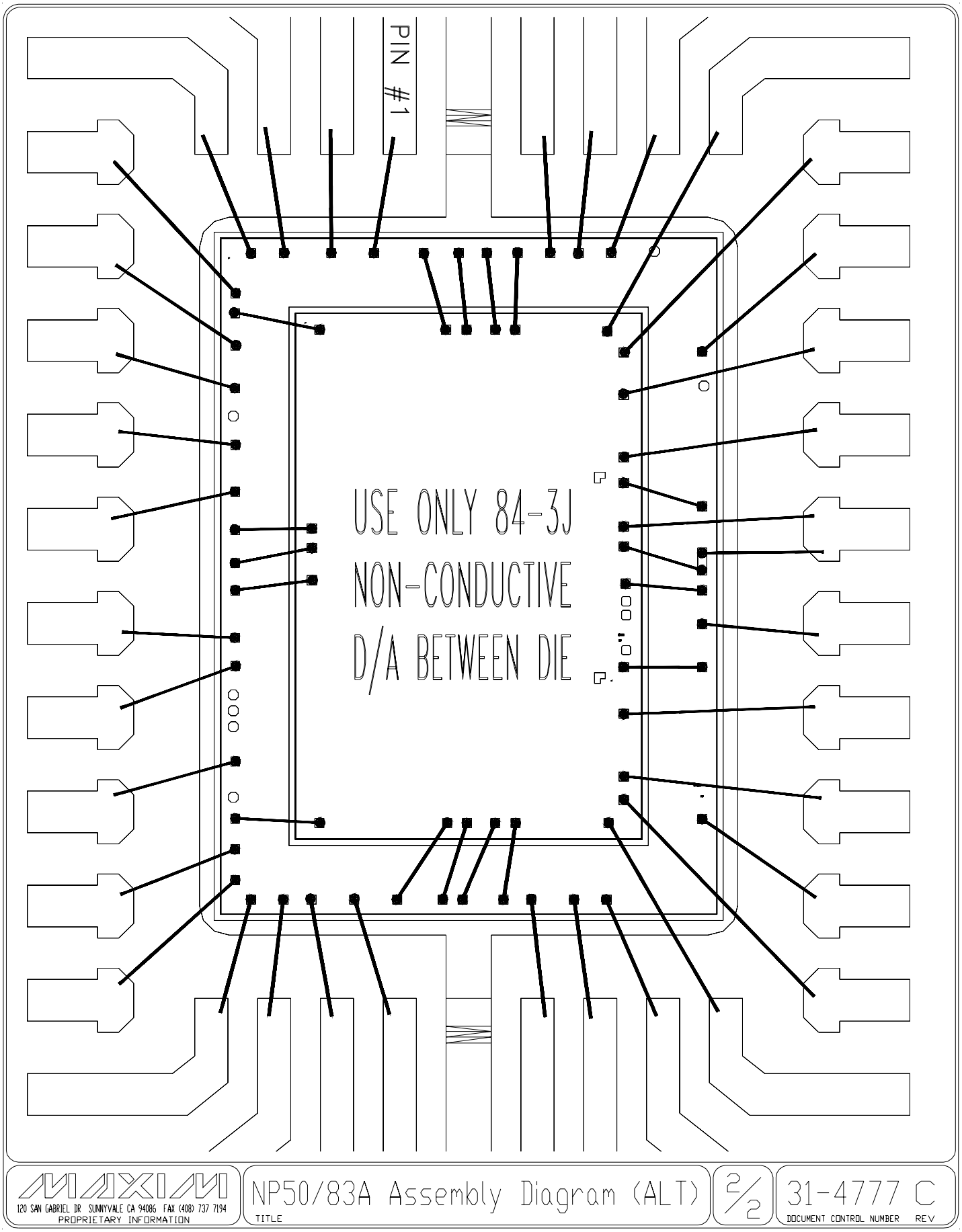
NP50/83A Assembly Diagram

TITLE

1/2

31-4777 C

DOCUMENT CONTROL NUMBER REV



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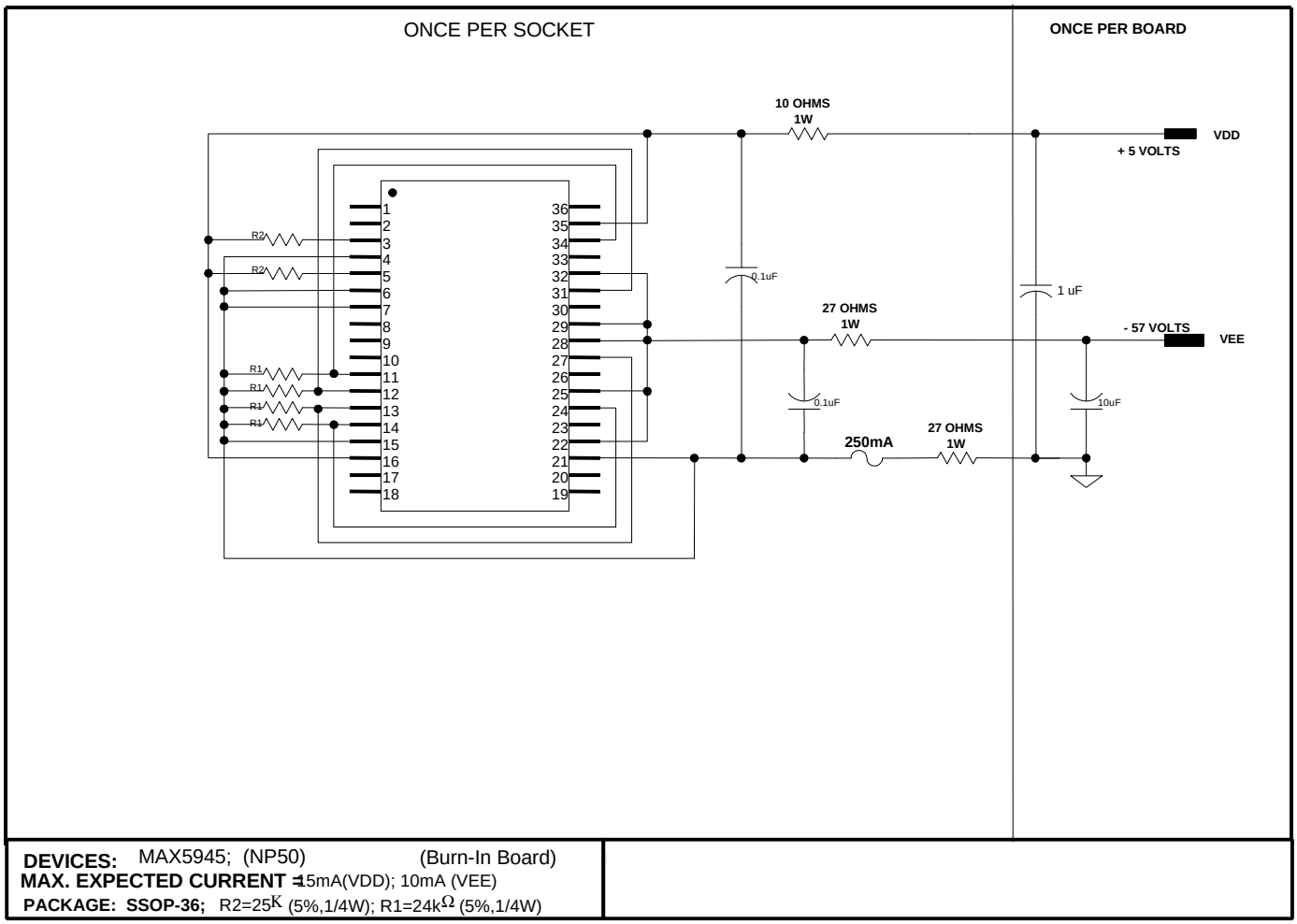
NP50/83A Assembly Diagram (ALT)
TITLE

2/2

31-4777 C
DOCUMENT CONTROL NUMBER REV



DEVICES: MAX5945; (NP50) (Burn-In Board)
MAX. EXPECTED CURRENT = 15mA(VDD); 10mA (VEE)
PACKAGE: SSOP-36; R2=25^{K} (5%,1/4W); R1=24k$^{\Omega}$ (5%,1/4W)

MAXIM	**TITLE:** BI Circuit: MAX5945 (NP50)		
	DOCUMENT I.D. 06-6162	**REVISION** B	**PAGE** 2