RELIABILITY REPORT

FOR

MAX5903xxEUT

PLASTIC ENCAPSULATED DEVICES

September 20, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by	Reviewed by
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Conclusion

The MAX5903 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5903 is a SOT23 hot-swap controller that allows a circuit card to be safely hot plugged into a live backplane without causing a glitch on the power-supply rail. This device operates from +9V to +72V and provide the simplest hot-swap solution by eliminating all external components except the external P-channel MOSFET.

The MAX5903 limits the inrush current to the load and provides a circuit breaker function for overcurrent protection. During startup the circuit breaker function is disabled and the MAX5903 limits the inrush current by gradually turning on the external MOSFET. Once the external MOSFET is fully enhanced, the circuit breaker function is enabled and the MAX5903 provides overcurrent protection by monitoring the voltage drop across the external MOSFET's on-resistance. The MAX5903 includes an undervoltage lock-out (UVLO) function, ON/OFF control input and a power-good status output, PGOOD (MAX5903). A built in thermal shutdown feature is also included to protect the external MOSFET in case of overheating.

The MAX5903 offers latched or auto-retry fault management and is available with 300mV, 400mV or 500mV circuit breaker thresholds. The MAX5903 is available in a small SOT23 package, and is specified for the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltage (with respect to GND unless otherwise noted)	
VS, DRAIN, PGOOD, PGOOD	-0.3V to +76V
ON/OFF	-0.3V to +4V
GATE to VS	-12V to +0.3V
Current into any Pin	±3mA
Continuous Power Dissipation (TA = +70C)	
6-PIN SOT23	727mW
Derates above +70°C	
6-PIN SOT23	9.1mW/°C
Maximum Junction Temperature	+150C
Storage Temperature Range	-60C to +150C
Lead Temperature	Note 1

Note 1: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of solder profiles recommended in the industry standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

II. Manufacturing Information

A. Description/Function: +72V SOT23 Simple Swapper Hot-Swap Controller

B. Process: SG3 (Standard 3 micron silicon gate CMOS)

C. Number of Device Transistors: 658

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: April, 2001

III. Packaging Information

A. Package Type: **6-Pin SOT23 Flip-Chip**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: N/A

E. Bondwire: 6 mil dia. ball

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-1301-0020

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 45 X 90 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:
Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level:
0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } \underset{\uparrow}{4389} \text{ x } 80 \text{ x } 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \text{ x } 10^{-9}$

λ = 13.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5764) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The NP11-10 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±150mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX5903xxEUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

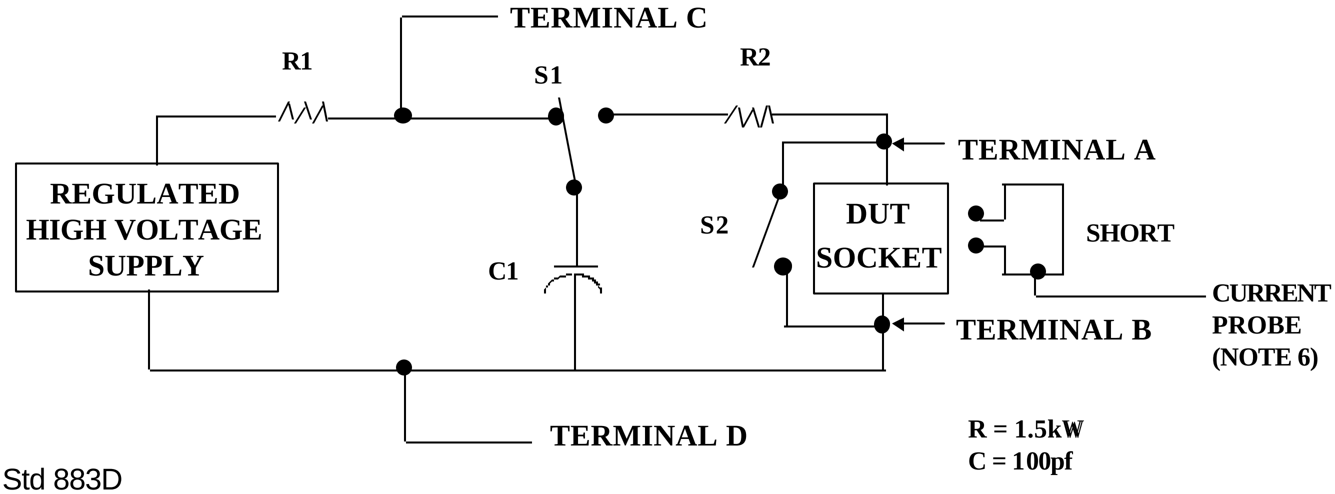
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

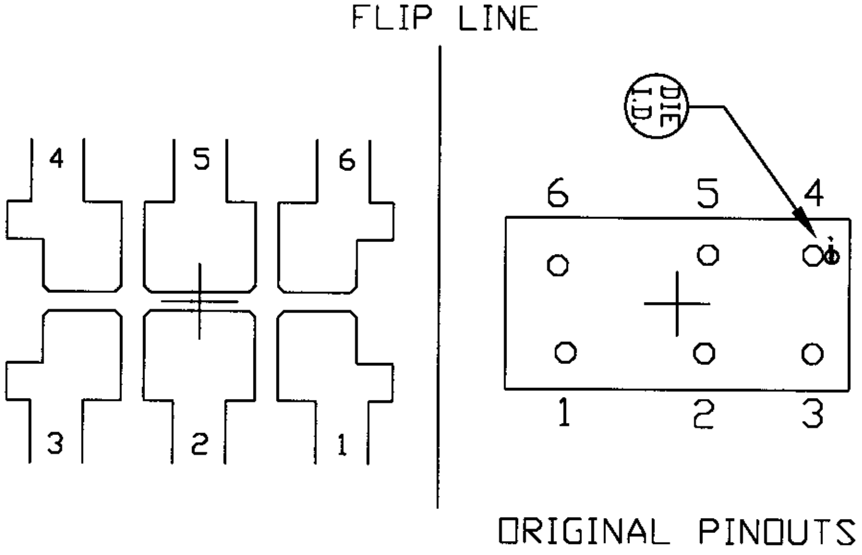
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

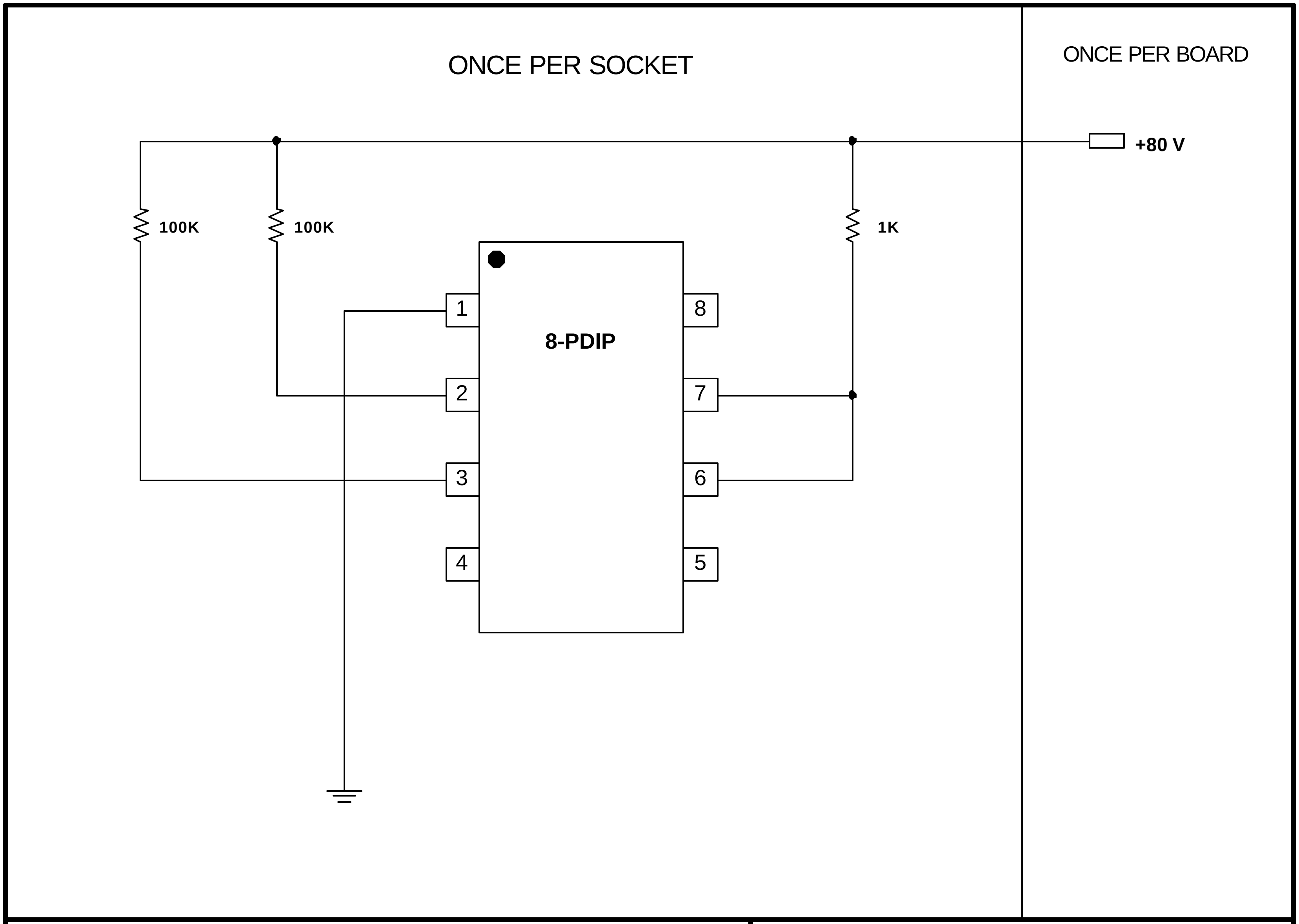


FLIP CHIP PKG.



NOTE: CAVITY DOWN

PKG. CODE: U6F-6		SIGNATURES	DATE	CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: FLIP CHIP	PKG. DESIGN			BOND DIAGRAM #: 05-1301-0020	REV: A



DEVICES: MAX 5902/5903

MAX. EXPECTED CURRENT = 4mA

DRAWN BY: TEK TAN

NOTES: