RELIABILITY REPORT

FOR

MAX5894EGK+

PLASTIC ENCAPSULATED DEVICES

February 4, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX5894EGK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX5894 programmable interpolating, modulating, 500Msps, dual digital-to-analog converter (DAC) offers superior dynamic performance and is optimized for high-performance wideband, single-carrier transmit applications. The device integrates a selectable 2x/4x/8x interpolating filter, a digital quadrature modulator, and dual 14-bit, high-speed DACs on a single integrated circuit. At 30MHz output frequency and 500Msps update rate, the in-band SFDR is 86dBc while consuming 1.1W. The device also delivers 73dB ACLR for two-carrier WCDMA at a 61.44MHz output frequency.

The selectable interpolating filters allow lower input data rates while taking advantage of the high DAC update rates. These linear-phase interpolation filters ease reconstruction filter requirements and enhance the passband dynamic performance. Individual offset and gain programmability allow the user to calibrate out local oscillator (LO) feedthrough and sideband suppression errors generated by analog quadrature modulators.

The MAX5894 features a fIM/4 digital image-reject modulator. This modulator generates a quadrature-modulated IF signal that can be presented to an analog I/Q modulator to complete the upconversion process. A second digital modulation mode allows the signal to be frequency-translated with image pairs at fIM/2 or fIM/4.

The MAX5894 features a standard 1.8V CMOS, 3.3V tolerant data input bus for easy interface. A 3.3V SPI™ port is provided for mode configuration. The programmable modes include the selection of 2x/4x/8x interpolating filters, fIM/2, fIM/4 or no digital quadrature modulation with image rejection, channel gain and offset adjustment, and offset binary or two's complement data interface.

Pin-compatible 12- and 16-bit devices are also available. Refer to the MAX5893 data sheet for the 12-bit version and the MAX5895 data sheet for the 16-bit version.

II. Manufacturing Information

A. Description/Function:	14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea
F. Date of Initial Production:	4/21/2005

III. Packaging Information

A. Package Type:	68-pin QFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2724
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	24°C/W
M. Multi Layer Theta Jc:	0.8°C/W

IV. Die Information

A. Dimensions:	179 X 184 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.2 \times 10^{-9}$

λ = 11.2 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CD08-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-800 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1

Reliability Evaluation Test Results

MAX5894EGK+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	96	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data