MAX5886EGK
Rev. A

RELIABILITY REPORT

FOR

**MAX5886EGK**

PLASTIC ENCAPSULATED DEVICES

September 9, 2003

# MAXIM INTEGRATED PRODUCTS


120 SAN GABRIEL DR.

SUNNYVALE, CA 94086



Written by

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## Conclusion

The MAX5886 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

A. General

The MAX5886 is an advanced, 12-bit, 500Msps digital-to-analog converter (DAC) designed to meet the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from a single 3.3V supply, this DAC offers exceptional dynamic performance such as 76dBc spurious-free dynamic range (SFDR) at $f_{OUT}$ = 30MHz. The DAC supports update rates of 500Msps and a power dissipation of only 230mW.

The MAX5886 utilizes a current-steering architecture, which supports a full-scale output current range of 2mA to 20mA, and allows a differential output voltage swing between $0.1V_{P-P}$ and $1V_{P-P}$.

The MAX5886 features an integrated 1.2V bandgap reference and control amplifier to ensure high accuracy and low noise performance. Additionally, a separate reference input pin enables the user to apply an external reference source for optimum flexibility and to improve gain accuracy.

The digital and clock inputs of the MAX5886 are designed for differential low-voltage differential signal (LVDS)-compatible voltage levels. The MAX5886 is available in a 68-pin QFN package with an exposed paddle (EP) and is specified for the extended industrial temperature range (-40°C to +85°C).

B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| AVDD, DVDD, VCLK to AGND | -0.3V to +3.9V |
| AVDD, DVDD, VCLK to DGND | -0.3V to +3.9V |
| AVDD, DVDD, VCLK to CLKGND | -0.3V to +3.9V |
| AGND, CLKGND to DGND | -0.3V to +0.3V |
| DACREF, REFIO, FSADJ to AGND | -0.3V to AVDD + 0.3V |
| IOUTP, IOUTN to AGND | -1V to AVDD + 0.3V |
| CLKP, CLKN to CLKGND | -0.3V to VCLK + 0.3V |
| B0P/B0N–B11P/B11N, SEL0, PD to DGND | -0.3V to DVDD + 0.3V |
| Thermal Resistance (?JA) | +24°C/W |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 68-Pin QFN | 3333mW |
| Derates above +70°C | |
| 68-Pin QFN | 41.7mW/°C |

## II. Manufacturing Information

A. Description/Function: 3.3V, 12-Bit, 500Msps High Dynamic Performance DAC with Differential LVDS Inputs

B. Process: TC35 (.35 Micron CMOS)

C. Number of Device Transistors: 10,629

D. Fabrication Location: Taiwan

E. Assembly Location: Korea

F. Date of Initial Production: April, 2003

## III. Packaging Information

A. Package Type: **68-Pin QFN (10 x 10)**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-9000-0001

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 3

## IV. Die Information

A. Dimensions: 116 x 134 mils

B. Passivation: $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: Metal 1 = 0.5 / Metal 2 = 0.6 / Metal 3 = 0.6 microns (as drawn)

F. Minimum Metal Spacing: Metal 1 = 0.45 / Metal 2 = 0.5 / Metal 3 = 0.6 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: $SiO_2$

I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 135 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV (applies to the factor 4389)

$\lambda = 8.04 \times 10^{-9}$

$\lambda$ = 8.04 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-7052) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The CD03-2 die type has been found to have all pins able to withstand a transient pulse of ±2500V Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX5886EGK**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 135 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | QFN | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

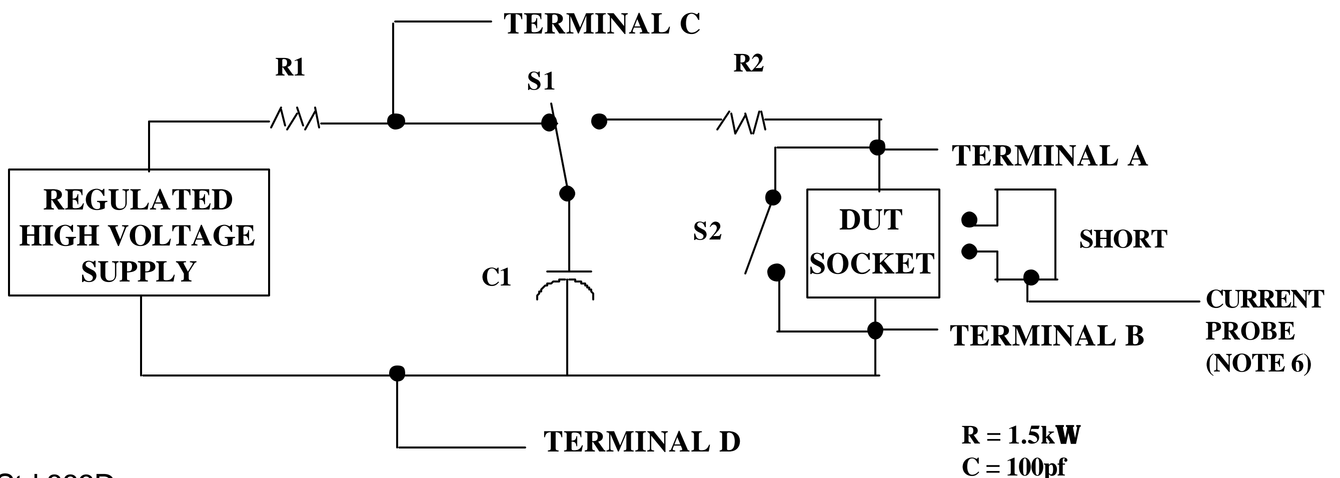
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

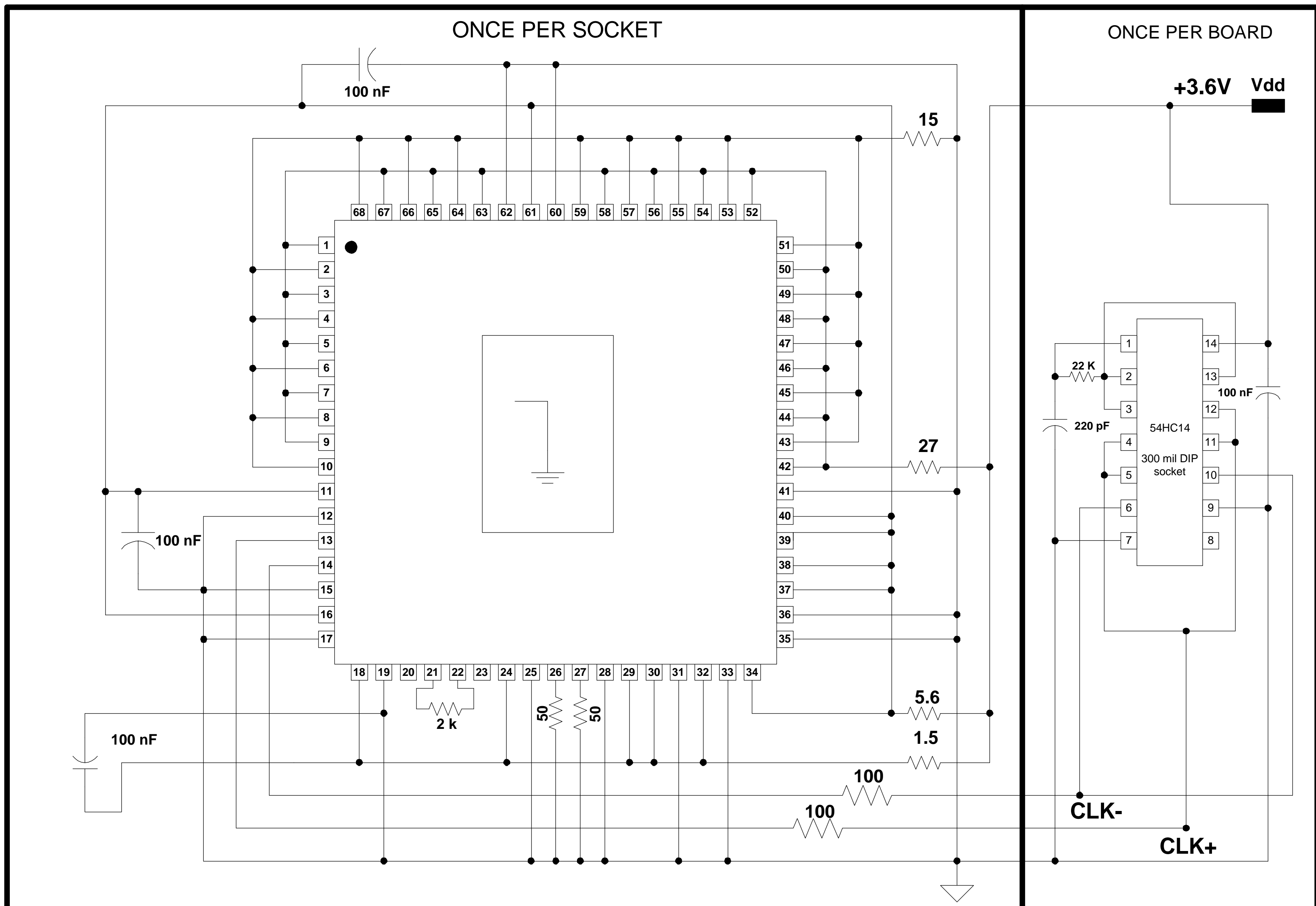
51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35

DIE I.D.

18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34

PKG. BODY SIZE: 10x10 mm

EXPOSED PAD PKG.




**DEVICES: MAX 5886/87/88 (CD03)**

**PACKAGE: 68-QFN (10x10x0.85mm, 0.5mm pitch)**

**MAX. EXPECTED CURRENT = 98 mA**

**DRAWN BY: TEK TAN / TODD BEJSOVEC**

**NOTES:** CLK+ and CLK- are inverse of each other. CLK+/- = 200 Khz, 1.5-2.5v. 54HC14 inserted in the 14-pin 300 mil DIP socket. Exposed pad should be GND.