RELIABILITY REPORT

FOR

MAX5885EGM+D

PLASTIC ENCAPSULATED DEVICES

July 19, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX5885EGM+D successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5885 is an advanced, 16-bit, 200Msps digital to-analog converter (DAC) designed to meet the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from a single 3.3V supply, this DAC offers exceptional dynamic performance such as 77dBc spurious-free dynamic range (SFDR) at fOUT = 10MHz. The DAC supports update rates of 200Msps at a power dissipation of less than 200mW. The MAX5885 utilizes a current-steering architecture, which supports a full-scale output current range of 2mA to 20mA, and allows a differential output voltage swing between 0.1VP-P and 1VP-P. The MAX5885 features an integrated 1.2V bandgap reference and control amplifier to ensure high accuracy and low noise performance. Additionally, a separate reference input pin enables the user to apply an external reference source for optimum flexibility and to improve gain accuracy. The digital and clock inputs of the MAX5885 are designed for CMOS-compatible voltage levels. The MAX5885 is available in a 48-pin QFN package with an exposed paddle (EP) and is specified for the extended industrial temperature range (-40°C to +85°C). See a parametric table of the complete family of pin-compatible, 12-/14-/16-bit high-speed DACs.

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II. Manufacturing Information

A. Description/Function:	3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea
F. Date of Initial Production:	April 23, 2003

III. Packaging Information

A. Package Type:	48-pin QFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0051
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	37°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	26°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	105 X 134 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 135 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 1.6 \times 10^{-9}$

λ = 1.6 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QM80BQ002A D/C 0251)

The CD04 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX5885EGM+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	45	0	QM80BQ002D, D/C 0512
	Biased	& functionality	45	0	QM80BQ002C, D/C 0512
	Time = 1000 hrs.		45	0	QM80BQ002B, D/C 0512

Note 1: Life Test Data may represent plastic DIP qualification lots.

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