RELIABILITY REPORT

FOR

MAX5873EGK+D

PLASTIC ENCAPSULATED DEVICES

October 10, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX5873EGK+D successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5873 is an advanced 12-bit, 200Msps, dual digital-to-analog converter (DAC). This DAC meets the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from 3.3V and 1.8V supplies, this dual DAC offers exceptional dynamic performance such as 78dBc spurious-free dynamic range (SFDR) at fOUT = 16MHz and supports update rates of 200Msps, with a power dissipation of only 255mW. The MAX5873 utilizes a current-steering architecture that supports a 2mA to 20mA full-scale output current range, and allows a 0.1VP-P to 1VP-P differential output voltage swing. The MAX5873 features an integrated 1.2V bandgap reference and control amplifier to ensure high-accuracy and low-noise performance. A separate reference input (REFIO) allows for the use of an external reference source for optimum flexibility and improved gain accuracy. The digital and clock inputs of the MAX5873 accept 3.3V CMOS voltage levels. The MAX5873 features a flexible input data bus that allows for dual-port input or a single-interleaved data port. The MAX5873 is available in a 68-pin QFN package with an exposed paddle (EP) and is specified for the extended temperature range (-40°C to +85°C). Refer to the MAX5874 and MAX5875 data sheets for pin-compatible 14-bit and 16-bit versions of the MAX5873, respectively. Refer to the MAX5876 for an LVDS-compatible version of the MAX5873. See a parametric table of the complete family of pin-compatible 12-/14-/16-bit high-speed DACs.

II. Manufacturing Information

A. Description/Function:	12-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea
F. Date of Initial Production:	October 21, 2004

III. Packaging Information

A. Package Type:	68-pin QFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0985
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	24°C/W
M. Multi Layer Theta Jc:	0.8°C/W

IV. Die Information

A. Dimensions:	153X143 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.45 \times 10^{-9}$

λ = 11.45 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot QFC5CQ003A, D/C 0438)

The CD05-5 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX5873EGK+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	QFC1BQ003A, D/C 0450
	Biased	& functionality	48	0	QFC5CQ003B, D/C 0505
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots