RELIABILITY REPORT

FOR

MAX5869EXE+

PLASTIC ENCAPSULATED DEVICES

February 11, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX5869EXE+ successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5869 high-performance interpolating and modulating 16-bit 5.9Gsps RF DAC can directly synthesize up to 600MHz of instantaneous bandwidth from DC to frequencies greater than 2.8GHz. The device is optimized for digital video broadcast and cable applications and meets spectral mask requirements for a broad set of communication standards including DVB-T, DVB-T2, DVB-C2, DVB-S2, DVB-S2X, ISDB-T, EPoC, and DOCSIS 3.0/3.1. The device integrates interpolation filters, a digital quadrature modulator, a numerically controlled oscillator (NCO), clock multiplying PLL+VCO and a 14-bit RF DAC core. The user-configurable 5x, 6x, 6.67x, 8x, 10x, 12x, 13.33x, 16x, 20x or 24x, linear phase interpolation filters simplify reconstruction filtering, while enhancing passband dynamic performance, and reduce the input data bandwidth required from an FPGA/ASIC. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis. The MAX5869 accepts 16-bit input data via a four-lane JESD204B SerDes data input interface that is Subclass-0 and Subclass-1 compliant. The interface can be configured for 1, 2, or 4 lanes and supports data rates up to 10Gbps per lane allowing flexibility to optimize the I/O count and speed. The MAX5869 clock input has a flexible clock interface and accepts a differential sine-wave, or square-wave input clock signal. A bypassable clock multiplying PLL and VCO can be used to generate a high-frequency sampling clock. The device outputs a divided reference clock to ensure synchronization of the system clock and DAC clock. In addition, multiple devices can be synchronized using JESD204B Subclass-1. The MAX5869 uses a differential current-steering architecture and can produce a 0dBm full-scale output signal level with a 50 load. Operating from 1.8V and 1.0V power supplies, the device consumes 2.5W at 4.9Gsps. The device is offered in a compact 144-pin, 10mm x 10mm, FCCSP package and is specified for the extended industrial temperature range (-40°C to +85°C).

II. Manufacturing Information

A. Description/Function:	16-Bit, 5.9Gsps Interpolating and Modulating RF DAC with JESD204B Interface
B. Process:	TS65
C. Number of Device Transistors:	6277468
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	March 27, 2015

III. Packaging Information

A. Package Type:	144-bump FCCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5591
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	16.2°C/W
M. Multi Layer Theta Jc:	2.5°C/W

IV. Die Information

A. Dimensions:	158.3464X173.2283 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.9 microns (as drawn)
F. Minimum Metal Spacing:	0.9 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 75 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.7 \times 10^{-9}$

λ = 14.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS65 Process results in a FIT Rate of 0.56 @ 25°C and 9.59 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The CD24-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5869EXE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	75	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.