RELIABILITY REPORT

FOR

MAX5590EUG
(MAX5590 – MAX5595)

PLASTIC ENCAPSULATED DEVICES

July 6, 2005

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Written by

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Conclusion

The MAX5590-95 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5590-95 octal, 8-bit, voltage-output digital-to-analog converter (DAC) offers buffered outputs and a 3µs maximum settling time at the 12-bit level. The DAC operates from a +2.7V to +5.25V analog supply and a separate +1.8V to +5.25V digital supply. The 20MHz 3-wire serial interface is compatible with SPI™, QSPI™, MICROWIRE™, and digital signal processor (DSP) protocol applications. Multiple devices can share a common serial interface in direct-access or daisy-chained configuration. The MAX5590-95 provides two multifunction, user-programmable, digital I/O ports. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale. Software-selectable FAST and SLOW settling modes decrease settling time in FAST mode, or reduce supply current in SLOW mode.

The MAX5590-95 is an 8-bit DAC providing forcesense- configured output buffers. The MAX5590-95 is specified over the extended -40°C to +85°C temperature range, and is available in a spacesaving 24-pin TSSOP package

B. Absolute Maximum Ratings

Item	Rating
AVDD to DVDD	±6V
AGND to DGND	±0.3V
AVDD to AGND, DGND	-0.3V to +6V
DVDD to AGND, DGND	-0.3V to +6V
FB_, OUT_, REF to AGND	-0.3V to the lower of (AVDD + 0.3V) or +6V
SCLK, DIN, CS, PU, DSP to DGND	-0.3V to the lower of (DVDD + 0.3V) or +6V
UPIO1, UPIO2 to DGND	-0.3V to the lower of (DVDD + 0.3V) or +6V
Maximum Current into Any Pin	±50mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin TSSOP	976mW
Derates above +70°C	
24-Pin TSSOP	12.2mW/°C

II. Manufacturing Information

A. Description/Function:	Buffered, Fast-Settling, Octal, 8-Bit, Voltage-Output DAC
B. Process:	C6Y (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors:	38,513
D. Fabrication Location:	Japan
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	October, 2003

III. Packaging Information

A. Package Type:	**24-Pin TSSOP**
B. Lead Frame:	Copper or 100% Matte Tin
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0420
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	108 x 192 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.91 \times 10^{-9}$

λ =22.91 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the C6Y Process results in a FIT Rate of 0.82 @ 25C and 14.21 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DB08-2 die type has been found to have all pins able to withstand a transient pulse of ±2000V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX5590-95EUG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.