RELIABILITY REPORT

FOR

MAX5591AEUI+T

PLASTIC ENCAPSULATED DEVICES

March 30, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX5591AEUI+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5590-MAX5595 octal, 12/10/8-bit, voltage-output digital-to-analog converters (DACs) offer buffered outputs and a 3µs maximum settling time at the 12-bit level. The DACs operate from a +2.7V to +5.25V analog supply and a separate +1.8V to +5.25V digital supply. The 20MHz 3-wire serial interface is compatible with SPI(tm), QSPI(tm), MICROWIRE(tm), and digital signal processor (DSP) protocol applications. Multiple devices can share a common serial interface in direct-access or daisy-chained configuration. The MAX5590-MAX5595 provide two multifunction, user-programmable, digital I/O ports. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale. Software-selectable FAST and SLOW settling modes decrease settling time in FAST mode, or reduce supply current in SLOW mode. The MAX5590/MAX5591 are 12-bit DACs, the MAX5592/MAX5593 are 10-bit DACs, and the MAX5594/MAX5595 are 8-bit DACs. The MAX5590/MAX5592/MAX5594 provide unity-gain-configured output buffers, while the MAX5591/MAX5593/MAX5595 provide force-sense-configured output buffers. The MAX5590-MAX5595 are specified over the extended -40°C to +85°C temperature range, and are available in space-saving 24-pin and 28-pin TSSOP packages.

II. Manufacturing Information

A. Description/Function:	Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs
B. Process:	C6Y
C. Number of Device Transistors:	38513
D. Fabrication Location:	Japan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	October 14, 2003

III. Packaging Information

A. Package Type:	28-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0421
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	78°C/W
K. Single Layer Theta Jc:	13°C/W
L. Multi Layer Theta Ja:	71.6°C/W
M. Multi Layer Theta Jc:	13°C/W

IV. Die Information

A. Dimensions:	108 X 192 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the C6Y Process results in a FIT Rate of 0.17 @ 25°C and 2.9 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The DB08-4 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5591AEUI+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.