RELIABILITY REPORT

FOR

MAX5556ESA+

PLASTIC ENCAPSULATED DEVICES

September 30, 2009

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

| **Approved by** |
|---|
| Ken Wendel |
| Quality Assurance |
| Director, Reliability Engineering |

**Conclusion**

The MAX5556ESA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

**Table of Contents**



**I. Device Description**

A. General

The MAX5556-MAX5559 stereo audio sigma-delta digital-to-analog converters (DACs) offer a simple and complete stereo digital-to-analog solution for media servers, set-top boxes, video-game hardware, automotive rear-seat entertainment and other general consumer audio applications. These DACs feature built-in digital interpolation/filtering, sigma-delta digital-to-analog conversion and analog output filtering. Control logic and mute circuitry minimize audible pops and clicks during power-up, power-down, clock changes, or when invalid clock conditions occur. The MAX5556-MAX5559 receive input data over a flexible 3-wire interface, supporting I²S-compatible, left-justified, right-justified 16-bit, and right-justified 18-bit audio data. Data can be clocked by either an external or internal serial clock. The internal serial clock frequency is programmable by selection of a master clock (MCLK) and sample clock (LRCLK) ratio. Sampling rates from 2kHz to 50kHz are supported. The MAX5556-MAX5559 operate from a single +4.75V to +5.5V analog supply with total harmonic distortion plus noise below -87dB. These devices are available in 8-pin SO packages and are specified over the -40°C to +85°C industrial temperature range.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Low-Cost Stereo Audio DACs |
| B. Process: | C6 |
| C. Number of Device Transistors: | 74109 |
| D. Fabrication Location: | California |
| E. Assembly Location: | Philippines, Thailand |
| F. Date of Initial Production: | April 22, 2006 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 8-pin SOIC (N) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive Epoxy |
| E. Bondwire: | Gold (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-1814 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 170°C/W |
| K. Single Layer Theta Jc: | 40°C/W |
| L. Multi Layer Theta Ja: | 128.4°C/W |
| M. Multi Layer Theta Jc: | 36°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 85 X 145 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Ken Wendel (Director, Reliability Engineering)<br>Bryan Preeshl (Managing Director of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 46 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.3 \times 10^{-9}$

$\lambda$ = 23.3 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DB24 die type has been found to have all pins able to withstand an ESD transient pulse of:

HBM: +/-2500 V per JESD22-A114

CDM: +/-750 V per JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

**Table 1**

Reliability Evaluation Test Results

**MAX5556ESA+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 46 | 0 |
| **Moisture Testing** (Note 2) | | | | |
| HAST | Ta = 130°C<br>RH = 85%<br>Biased<br>Time = 96hrs. | DC Parameters<br>& functionality | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data