

RELIABILITY REPORT FOR MAX5550ETE+T

PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

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Approved by
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Conclusion

The MAX5550ETE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

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The MAX5550 dual, 10-bit, digital-to-analog converter (DAC) features high-output-current capability. The MAX5550 sources up to 30mA per DAC, making it ideal for PIN diode biasing applications. Outputs can also be paralleled for high-current applications (up to 60mA typ). Operating from a single +2.7V to +5.25V supply, the MAX5550 typically consumes 1.5mA per DAC in normal operation and less than 1µA (max) in shutdown mode. The MAX5550 also features low output leakage current in shutdown mode (±1µA max) that is essential to ensure that the external PIN diodes are off. Additional features include an integrated +1.25V bandgap reference, and a control amplifier to ensure high accuracy and low-noise performance. A separate reference input (REFIN) allows for the use of an external reference source, such as the MAX6126, for improved gain accuracy. A pin-selectable I²C-/SPI(tm)-compatible serial interface provides optimum flexibility for the MAX5550. The maximum programmable output current value is set using software and an adjustment resistor. The MAX5550 is available in a (3mm × 3mm) 16-pin thin QFN package, and is specified over the extended (-40°C to +85°C) temperature range.



II. Manufacturing Information

- A. Description/Function:Dual, 10-Bit, Programmable, 30mA High-Output-Current DACB. Process:C6YC. Number of Device Transistors:8437
- D. Fabrication Location: Japan
- E. Assembly Location:Japan, ThailandF. Date of Initial Production:October 22, 2005

III. Packaging Information

A. Package Type:	16-pin Flip Chip TQFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	None
E. Bondwire:	N/A
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1768
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	57.2°C/W
M. Multi Layer Theta Jc:	40°C/W

IV. Die Information

Α.	Dimensions:	97 X 97 mils
В.	Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C.	Interconnect:	Al with Ti/TiN Barrier
D.	Backside Metallization:	None
E.	Minimum Metal Width:	0.6 microns (as drawn)
F.	Minimum Metal Spacing:	0.6 microns (as drawn)
G.	Bondpad Dimensions:	
Н.	Isolation Dielectric:	SiO ₂
Ι.	Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A.	Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
В.	Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C.	Observed Outgoing Defect Rate:	< 50 ppm
D.	Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \times 4340 \times 47 \times 2}$$
 (Chi square value for MTTF upper limit)

$$\lambda = 23.4 \times 10^{-9}$$

x = 23.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the C6Y Process results in a FIT Rate of 0.04 @ 25C and 0.73 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SIIAAQ001E, D/C 0533)

The DB25 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.



Table 1 Reliability Evaluation Test Results

MAX5550ETE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note	e 1) Ta = 135°C Biased	DC Parameters	47	0	SIIAAQ001B, D/C 0515
	Time = 192 hrs.	a functionality			

Note 1: Life Test Data may represent plastic DIP qualification lots.