RELIABILITY REPORT

FOR

MAX5541CSA+

PLASTIC ENCAPSULATED DEVICES

December 10, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

Conclusion

The MAX5541CSA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5541 serial-input, voltage-output, 16-bit monotonic digital-to-analog converter (DAC) operates from a single +5V supply. The DAC output is unbuffered, resulting in a low 0.3mA supply current and low 1 LSB offset error. The DAC output range is 0V to VREF. The DAC latch accepts a 16-bit serial word. A power-on reset (POR) circuit clears the DAC output to 0V (unipolar mode) when power is initially applied. The 10MHz 3-wire serial interface is SPI(tm)/QSPI(tm)/MICROWIRE(tm)-compatible and interfaces directly with optocouplers for applications requiring isolation. The MAX5541 is available in an 8-pin SO package. For the 1 LSB (max) INL version, refer to the MAX541 data sheet.

II. Manufacturing Information

A. Description/Function:	Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC
B. Process:	S12
C. Number of Device Transistors:	757
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Thailand, Philippines, Malaysia
F. Date of Initial Production:	October 22, 1999

III. Packaging Information

A. Package Type:	8-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0495
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	170°C/W
K. Single Layer Theta Jc:	40°C/W
L. Multi Layer Theta Ja:	128.4°C/W
M. Multi Layer Theta Jc:	36°C/W

IV. Die Information

A. Dimensions:	85X139 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.02 @ 25C and 0.33 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot NZFAC2015B, D/C 9938)

The DA58-1 die type has been found to have all pins able to withstand a HBM transient pulse of < 400V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX5541CSA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	NZFAC2015B, D/C 9938

Note 1: Life Test Data may represent plastic DIP qualification lots.