RELIABILITY REPORT

FOR

MAX547xxxH

PLASTIC ENCAPSULATED DEVICES

August 3, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX547 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX547 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). On-chip precision output amplifiers provide the voltage outputs. The MAX547 operates from a ±5V supply. Bipolar output voltages with up to ±4.5V voltage swing can be achieved with no external components. The MAX547 has four separate reference inputs; each is connected to two DACs, providing different full-scale output voltages for every DAC pair.

The MAX547 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous load (LD_-bar) input transfers data from the input latch to the DAC latch. The four LD_-bar inputs each control two DACs, and all DAC latches can be updated simultaneously by asserting all LD_-bar pins. An asynchronous clear (CLR-bar) input resets the output of all eight DACs to AGND_. Asserting CLR-bar resets both the DAC and the input latch to bipolar zero (1000hex). On power-up, reset circuitry performs the same function as CLR-bar. All logic inputs are TTL/CMOS compatible.

The MAX547 is available in 44-pin plastic quad flat pack and 44-pin PLCC packages.

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	-0.3V to +6V
VSS to GND	-6V to +0.3V
Digital Input Voltage to GND	-0.3V to (VDD + 0.3V)
REF_	(AGND_ - 0.3V) to (VDD + 0.3V)
AGND_	(VSS - 0.3V) to (VDD + 0.3V)
VOUT_	VDD to VSS
Maximum Current into REF_ Pin	±10mA
Maximum Current into Any Other Signal Pin	±50mA
Continuous Power Dissipation (TA = +70°C)	
PLCC (derate 13.33mW/°C above +70°C)	1067mW
Plastic FP (derate 11.11mW/°C above +70°C)	889mW
Operating Temperature Ranges	
MAX547–C–H	0°C to +70°C
MAX547–E–H	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

II. Manufacturing Information

A. Description/Function:	Octal, 13-Bit Voltage-Output DAC with Parallel Interface
B. Process:	S3 - Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	10,973
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	May, 1994

III. Packaging Information

A. Package Type:	**44 PLCC**	**44 Plastic FP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0401-0391	# 05-0401-0411
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 3	Level 3

IV. Die Information

A. Dimensions:	199 x 242 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 560 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 1.96 \times 10^{-9}$ λ = 1.96 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5042) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S3 Process results in a FIT Rate of 0.15 @ 25C and 2.60 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA52 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX547xxxH

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		560	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PLCC Plastic FP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

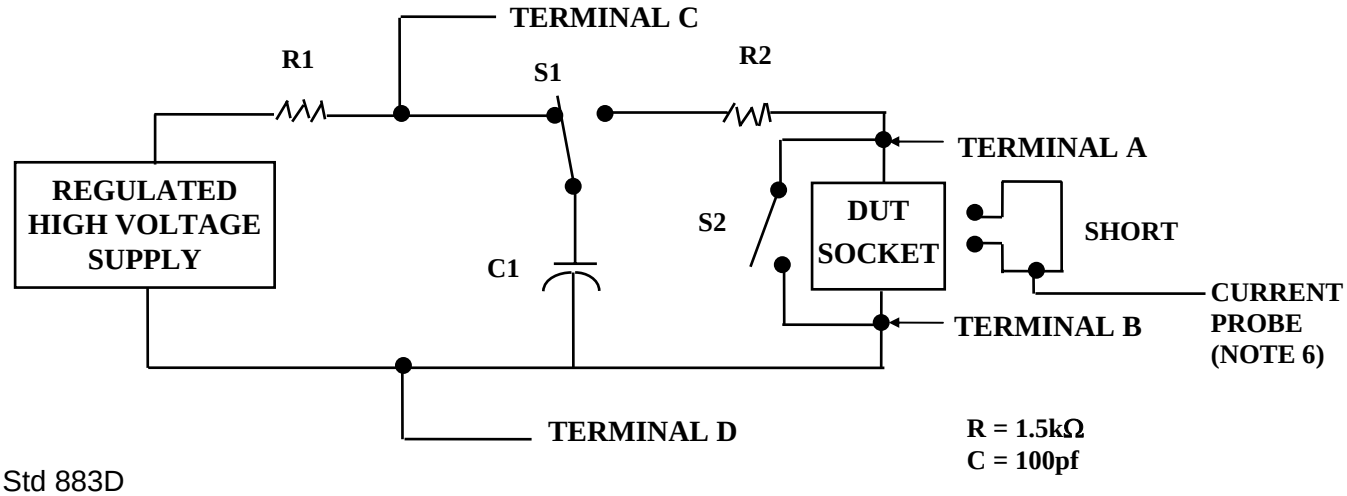
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

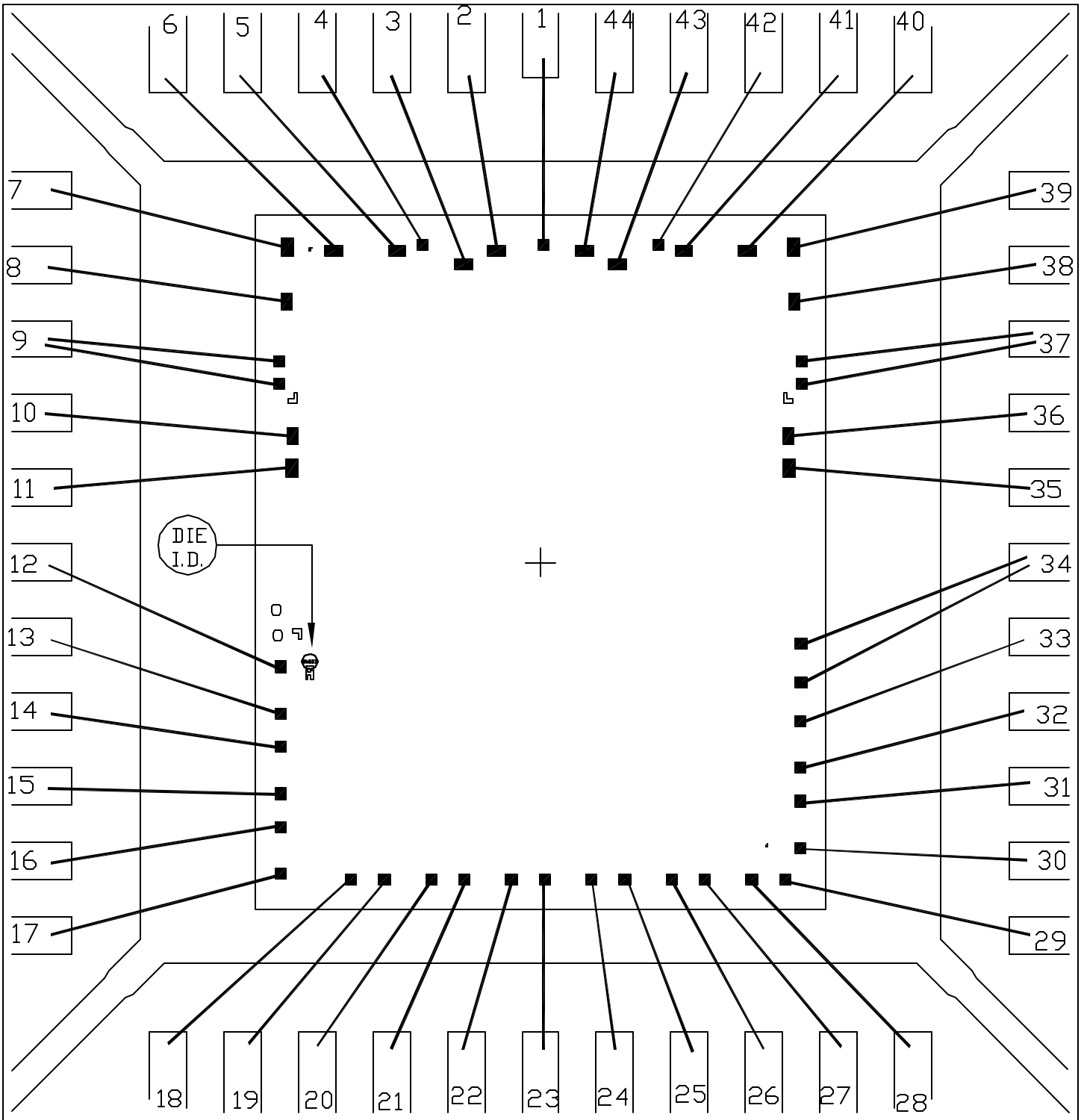
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

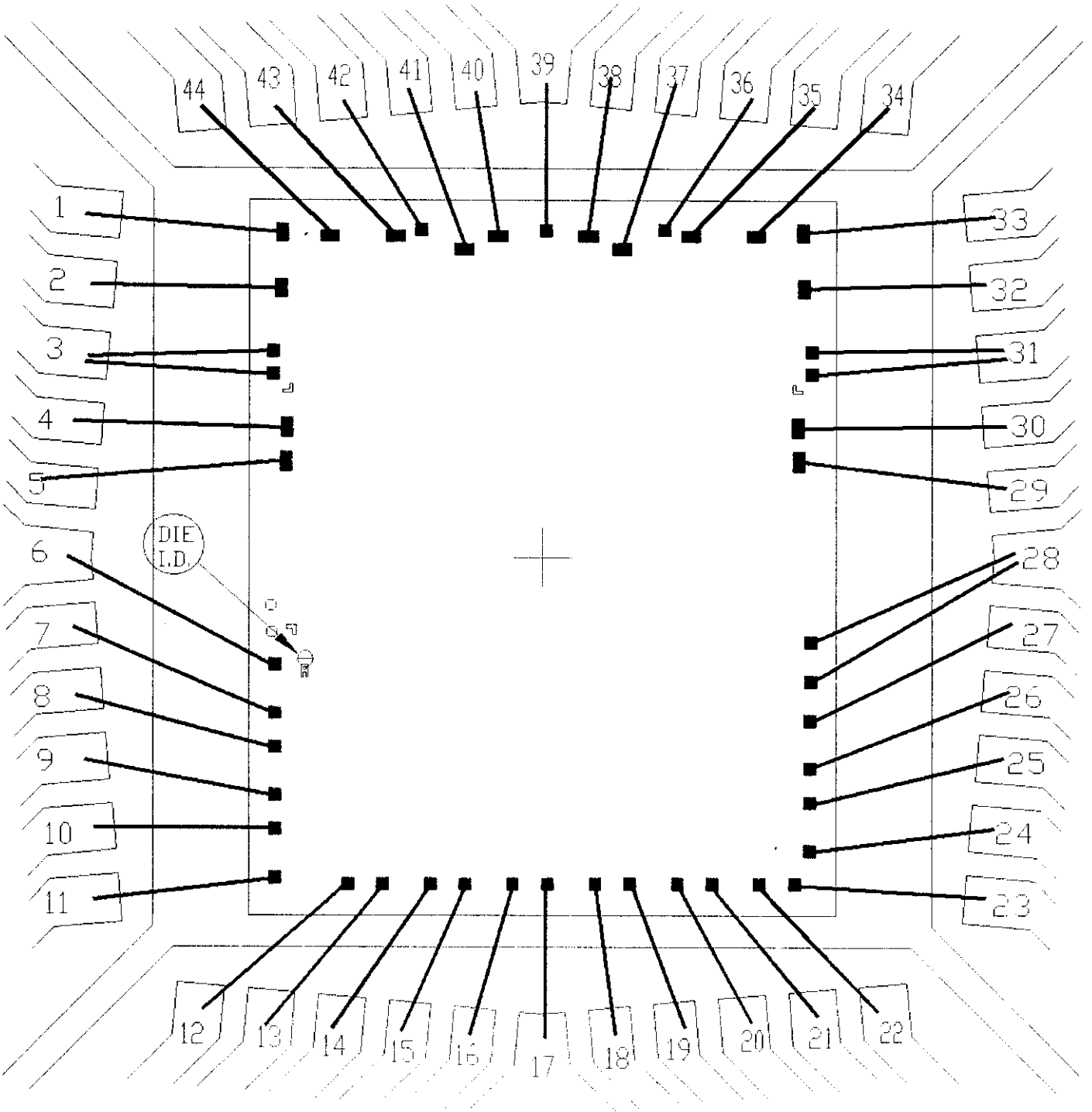
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

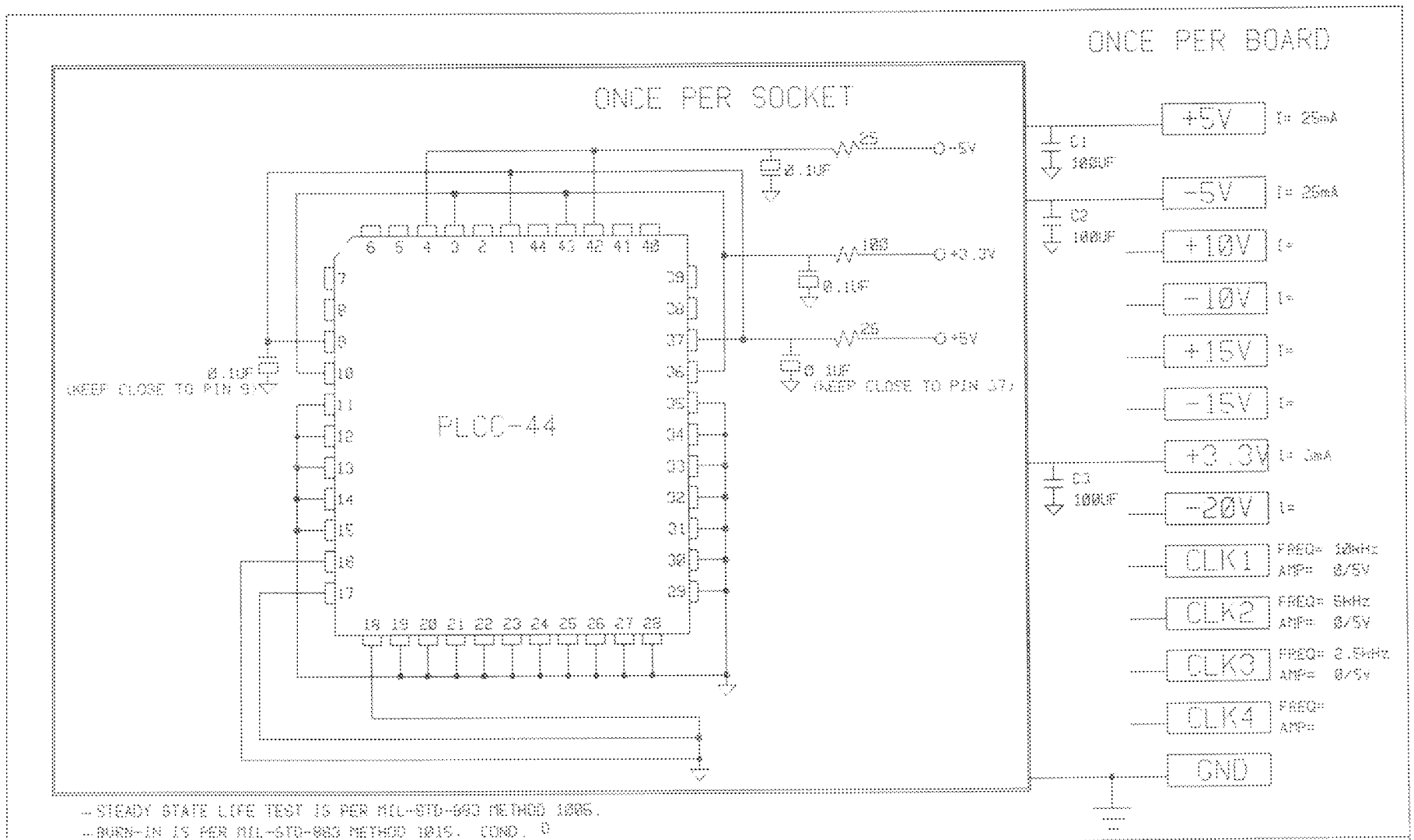




PKG. CODE: Q44-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 280X280	PKG.			BOND DIAGRAM #: 05-0401-0391	REV: B
	DESIGN				



PKG.CODE: M44-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 264X264	PKG. DESIGN			BUILDSHEET NUMBER: 05-0401-0411 REV.: A



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. D

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MIL/883C

SPEC. NO. 06-5042 REV. B

DATE: 1/5/94

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:

MAX547