

RELIABILITY REPORT
FOR
MAX5387MAUD+
PLASTIC ENCAPSULATED DEVICES

January 18, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX5387MAUD+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX5387 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10k , 50k , and 100k . Operating from a single +2.6V to +5.5V power supply, this device provides a low, 35ppm/°C end-to-end temperature coefficient. The device features an I²C interface. The small package size, low supply operating voltage, low supply current, and automotive temperature range of the MAX5387 make the device uniquely suitable for the portable consumer market, battery backup industrial applications, and the automotive market. The MAX5387 is specified over the automotive -40°C to +125°C temperature range and is available in a 14-pin TSSOP package.

II. Manufacturing Information

A. Description/Function:	Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer
B. Process:	S45
C. Number of Device Transistors:	20059
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	January 22, 2010

III. Packaging Information

A. Package Type:	14-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3699
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	30°C/W
L. Multi Layer Theta Ja:	100.4°C/W
M. Multi Layer Theta Jc:	30°C/W

IV. Die Information

A. Dimensions:	62 X 71 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- | | |
|-----------------------------------|--|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 96 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 11.4 \times 10^{-9}$$

$$\lambda = 11.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SVZZCQ001E D/C 0932)

The DP35-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX5387MAUD+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	48	0	SVZXCQ001A, D/C 0932
	Biased	& functionality	48	0	SVZYAQ001A, D/C 0912
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.