MAX5385ExT Rev. A

**RELIABILITY REPORT** 

FOR

### MAX5385ExT

PLASTIC ENCAPSULATED DEVICES

November 1, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Jim Pedicord Quality Assurance Reliability Lab Manager

Reviewed by

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Bryan J. Preeshl Quality Assurance Executive Director

### Conclusion

The MAX5385 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

### A. General

The MAX5385 low-cost, 8-bit digital-to-analog converter (DAC) in a miniature 6-pin SOT23 packages has a simple 3wire, SPI™/QSPI™/MICROWIRE™-compatible serial interface that operates up to 10MHz. The MAX5385 operates over the full +2.7V to +5.5V supply range and has an internal reference equal to 0.9 x V<sub>DD</sub>.

The MAX5385 requires an extremely low supply current of only 150µA (typ) and provides a buffered voltage output. This device powers up at zero code and remain there until a new code is written to the DAC registers. This provides additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5385 includes a 1µA, low-power shutdown mode that features software-selectable output loads of 1k $\Omega$ , 100k $\Omega$ , or 1M $\Omega$  to ground.

### B. Absolute Maximum Ratings

ltem	Rating
VDD to GND OUT CS, SCLK, DIN to GND Maximum Current into Any Pin Operating Temperature Range	-0.3V to +6V -0.3V to (VDD + 0.3V) -0.3V to +6V 50mA -40°C to +85°C
Storage Temperature Range Maximum Junction Temperature Lead Temperature (soldering, 10s)	-65°C to +150°C +150°C +300°C
Continuous Power Dissipation (TA = +70°C) 6-Pin SOT23 Derates above +70°C 6-Pin SOT23	696mW 8.7mW/°C

### II. Manufacturing Information

A. Description/Function:	Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23
B. Process:	S6 (0.6 micron CMOS)
C. Number of Device Transistors:	2160
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	July, 2000

# III. Packaging Information

A. Package Type:	6-Lead SOT23	6-Lead Thin SOT23
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0401-0523	# 05-0401-0567
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

### **IV. Die Information**

A. Dimensions:	57 x 35 mils mils
B. Passivation:	$Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si (Aluminum/ Silicon)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

### V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

### VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \text{ x } 4389 \text{ x } 321 \text{ x } 2}$$
 (Chi square value for MTTF upper limit)  
Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 3.38 \times 10^{-9}$$
  $\lambda = 3.38$  F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-5495) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The DA78-2 die type has been found to have all pins able to withstand a transient pulse of  $\pm 1500$ V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250$ mA.

# Table 1 Reliability Evaluation Test Results

MA	X5	38	5F	=x	Г
	<b>NJ</b>	30	J	_^	

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		321	0
Moisture Testin	g (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

# Attachment #1

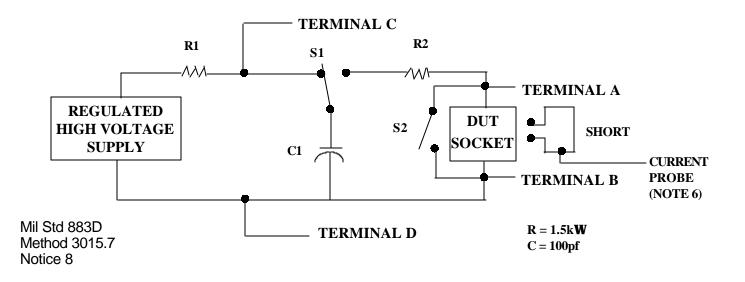
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V <sub>PS1</sub> <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

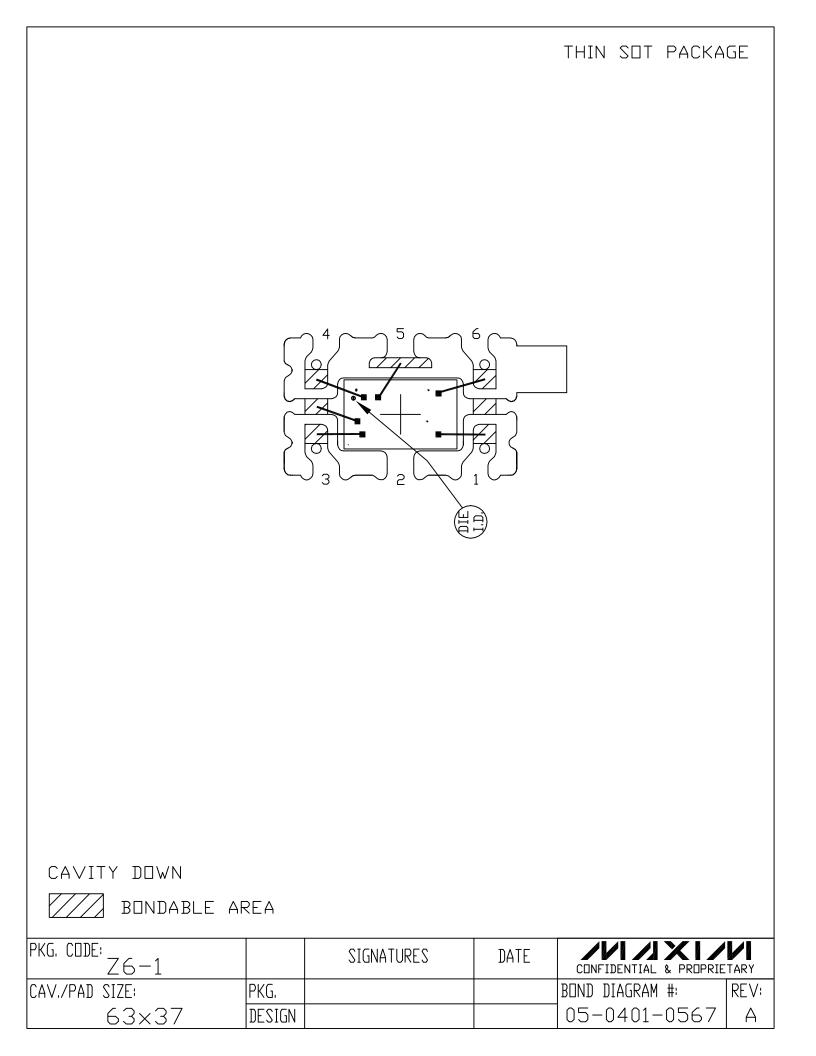
TABLE II. Pin combination to be tested. 1/2/

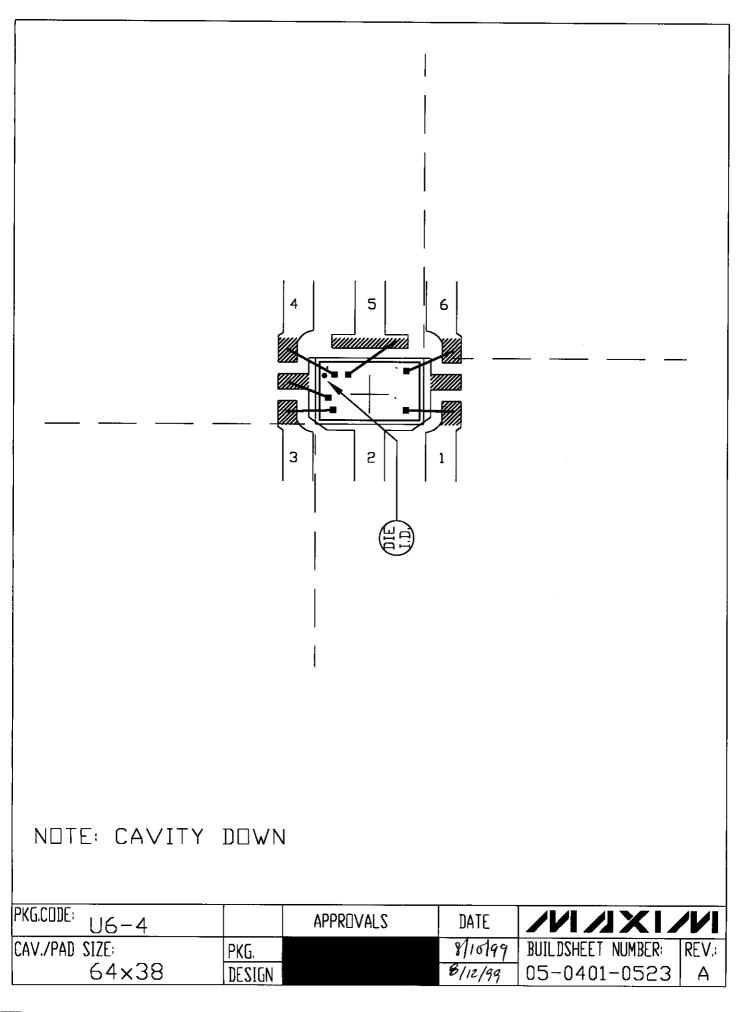
- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$  No connects are not to be tested.
- $\overline{3/}$  Repeat pin combination I for each named Power supply and for ground

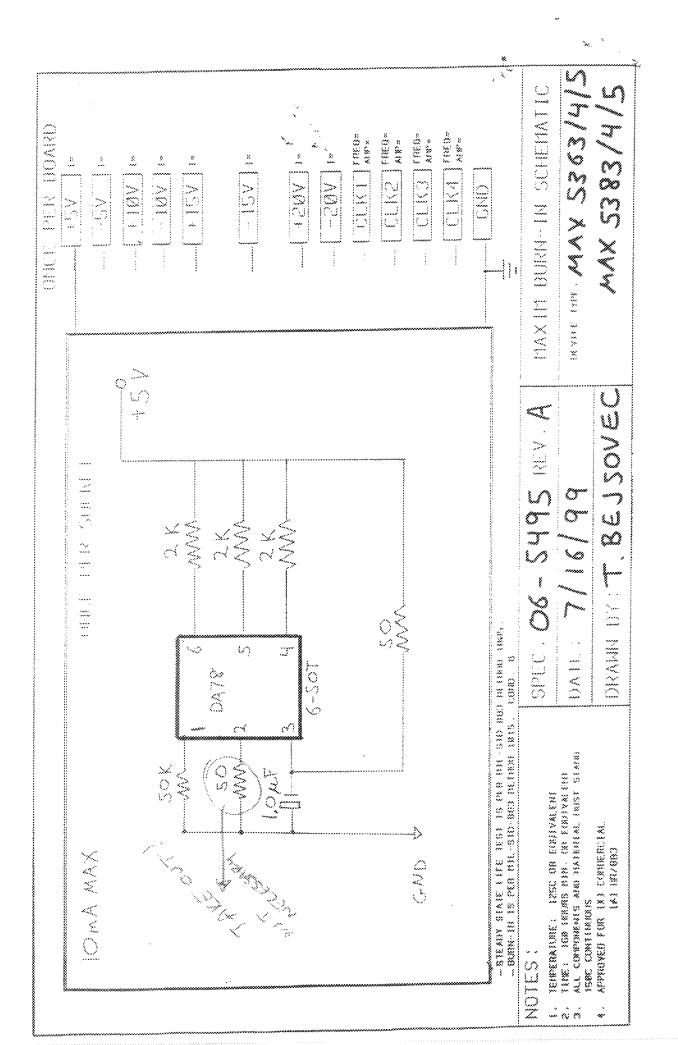
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND, + $V_{S}$ , - $V_{S}$ ,  $V_{REF}$ , etc).

- 3.4 <u>Pin combinations to be tested.</u>
  - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
  - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V<sub>SS1</sub>, or V<sub>SS2</sub> or V<sub>SS3</sub> or V<sub>CC1</sub>, or V<sub>CC2</sub>) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
  - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.









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