RELIABILITY REPORT

FOR

MAX5322EAI+

PLASTIC ENCAPSULATED DEVICES

February 5, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX5322EAI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX5322 dual, 12-bit, serial-interface, digital-to-analog converter (DAC) provides bipolar ±5V to ±10V outputs from ±12V to ±15V analog power-supply voltages, or unipolar 5V to 10V outputs from a single 12V to 15V analog power-supply voltage. The MAX5322 features excellent linearity with both integral nonlinearity (INL) and differential nonlinearity (DNL) guaranteed to ±1 LSB (max). The device also features a fast 10µs to 0.5 LSB settling time, and a hardware-shutdown feature that reduces current consumption to 2.8µA. The output goes to midscale at power-up in bipolar mode (0V), and to zero scale at power-up in unipolar mode (0V). A clear input (CLR-bar) asynchronously clears the DAC register and sets the outputs to 0V. The outputs can be asynchronously updated with the load DAC (LDAC-bar) input. The device features a fast 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial interface that operates with 3V or 5V logic. Additional features include a serialdata output (DOUT) for daisy chaining and read-back functions. The MAX5322 requires external reference voltages of 2V to 5.25V and is available in a 28-pin SSOP package that operates over the extended (-40°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	±10V, Dual, 12-Bit, Serial, Voltage-Output DAC
B. Process:	HV3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines
F. Date of Initial Production:	February 19, 2004

III. Packaging Information

A. Package Type:	28-pin SSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0438
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	105°C/W
K. Single Layer Theta Jc:	23.9°C/W
L. Multi Layer Theta Ja:	66.6°C/W
M. Multi Layer Theta Jc:	23°C/W

IV. Die Information

A. Dimensions:	145 X 260 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

λ = 22.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the HV3 Process results in a FIT Rate of 0.10 @ 25C and 1.77 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DB01 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1

Reliability Evaluation Test Results

MAX5322EAI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data