RELIABILITY REPORT

FOR

MAX5318GUG+T

PLASTIC ENCAPSULATED DEVICES

June 28, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX5318GUG+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5318 is a high-accuracy, 18-bit, serial SPI input, buffered voltage output digital-to-analog converter (DAC) in a 4.4mm x 7.8mm, 24-lead TSSOP package. The device features ±2 LSB INL (max) accuracy and a ±1 LSB DNL (max) accuracy over the full temperature range of -40°C to +105°C. The DAC voltage output is buffered resulting in a fast settling time of 3µs and a low offset and gain drift of ±0.5ppm/°C of FSR (typ). The force-sense output (OUT) maintains accuracy while driving loads with long lead lengths. Additionally, a separate AVSS supply, allows the output amplifier to go to 0V (GND) while maintaining full linearity performance. The MAX5318 includes user-programmable digital gain and offset correction to enable easy system calibration. At power-up, the device resets its outputs to zero or midscale. The wide 2.7V to 5.5V supply voltage range and integrated low-drift, low-noise reference buffer amplifier make for ease of use. The MAX5318 features a 50MHz, 3-wire, SPI interface. The MAX5318 is available in a 24-lead TSSOP package and operates over the -40°C to +105°C temperature range.

II. Manufacturing Information

A. Description/Function:	18-Bit, High-Accuracy Voltage Output DAC with Digital Gain, Offset Control, and SPI Interface
B. Process:	S45
C. Number of Device Transistors:	106927
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia, Thailand, Philippines
F. Date of Initial Production:	September 27, 2012

III. Packaging Information

A. Package Type:	24-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Bondwire:	Au (1.3 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-9000-4931
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	82°C/W
J. Single Layer Theta Jc:	15°C/W
K. Multi Layer Theta Ja:	72°C/W
L. Multi Layer Theta Jc:	13°C/W

IV. Die Information

A. Dimensions:	104X144 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
E. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G.Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The DB70 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX5318GUG+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.