RELIABILITY REPORT

FOR

MAX5312EAE+

PLASTIC ENCAPSULATED DEVICES

August 9, 2012

MAXIM INTEGRATED PRODUCTS

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Approved by
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Conclusion

The MAX5312EAE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5312 12-bit, serial-interface, digital-to-analog converter (DAC) provides bipolar ±5V to ±10V outputs from ±12V to ±15V power-supply voltages, or a unipolar 5V to 10V output from a single 12V to 15V power-supply voltage. The MAX5312 features excellent linearity with both integral nonlinearity (INL) and differential nonlinearity (DNL) guaranteed to ±1 LSB (max). The device also features a fast 10µs to 0.5 LSB settling time, and a hardware-shutdown feature that reduces current consumption to 3.5µA. The output goes to midscale at power-up in bipolar mode (0V), and to zero scale at power-up in unipolar mode (0V). A clear input (active-low CLR) asynchronously clears the DAC register and sets the output to 0V. The output can be asynchronously updated with the load DAC (active-low LDAC) input. The device features a 10MHz SPI(tm)-/QSPI(tm)-/MICROWIRE(tm)-compatible serial interface that operates with 3V or 5V logic. Additional features include a serial-data output (DOUT) for daisy chaining and read-back functions. The MAX5312 requires a 2V to 5.25V external reference voltage and is available in a 16-pin SSOP package that operates over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	±10V, 12-Bit, Serial, Voltage-Output DAC
B. Process:	HV3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines
F. Date of Initial Production:	January 16, 2004

III. Packaging Information

A. Package Type:	16L SSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0431 / B
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	140°C/W
K. Single Layer Theta Jc:	34°C/W
L. Multi Layer Theta Ja:	86°C/W
M. Multi Layer Theta Jc:	33°C/W

IV. Die Information

A. Dimensions:	163 X 144 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:Wafer	Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.4 \times 10^{-9}$

$\lambda = 4.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the HV3 Process results in a FIT Rate of 0.10 @ 25C and 1.77 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NEN0DQ001C D/C 0344)

The DA00 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX5312EAE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	48	0	NEN0DQ003B, D/C 0528

Note 1: Life Test Data may represent plastic DIP qualification lots.