RELIABILITY REPORT

FOR

MAX525xCxP

PLASTIC ENCAPSULATED DEVICES

August 1, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Written by

Jim Pedicord Quality Assurance Reliability Lab Manager Reviewed by

Bryan J. Preeshl Quality Assurance Executive Director

Conclusion

The MAX525 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description

II.Manufacturing Information

III.Packaging Information

IV.Die Information

V.Reliability Evaluation

VI.Reliability Evaluation

VI.Reliability Evaluation

I. Device Description

A. General

The MAX525 combines four low-power, voltage-output, 12-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX525 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset which clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated via the 3-wire serial interface. All logic inputs are TTL/CMOS-logic compatible.

B. Absolute Maximum Ratings

<u>ltem</u>		Rating
VDD to AGND		-0.3V to +6V
VDD to DGND		-0.3V to +6V
AGND to DGND	±0.3V	
REFAB, REFCD to AGND		-0.3V to (VDD + 0.3V)
OUT_, FB_ to AGND		-0.3V to (VDD + 0.3V)
Digital Inputs to DGND		-0.3V to +6V
DOUT, UPO to DGND		-0.3V to (VDD + 0.3V)
Operating Temperature Ranges		
MAX525_C_P		0°C to +70°C
MAX525_E_P		-40°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (soldering, 10sec)		+300°C
Junction Temperature		+150°C
Continuous Power Dissipation (TA = +70°C)		
20-Pin PDIP		640mW
20-Pin SSOP		640mW
Derates above +70°C		
20-Pin PDIP		8.0mW/°C
20-Pin SSOP		8.0mW/°C

II. Manufacturing Information

A. Description/Function: Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

B. Process: S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS

C. Number of Device Transistors: 4337

D. Fabrication Location: Cailfornia or Oregon, USA

E. Assembly Location: Malaysia or Philippines

F. Date of Initial Production: July, 1996

III. Packaging Information

A. Package Type: 20-Lead SSOP 20-Lead PDIP

B. Lead Frame: Copper Copper

C. Lead Finish: Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-0401-0460 Buildsheet # 05-0401-0459

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard JESD22-A112: Level 1 Level 1

IV. Die Information

A. Dimensions: 124 x 153 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } 4389 \text{ x } 160 \text{ x } 2}$$
(Chi square value for MTTF upper limit)
$$\lambda = 6.79 \text{ x } 10^{-9}$$
Temperature Acceleration factor assuming an activation energy of 0.8eV
$$\lambda = 6.79 \text{ x } 10^{-9}$$

$$\lambda = 6.79 \text{ F.I.T. } (60\% \text{ confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec. # 06-5168) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA83 die type has been found to have all pins able to withstand a transient pulse of ± 2500 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1Reliability Evaluation Test Results

MAX525xCxP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testin	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP SSOP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.

Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

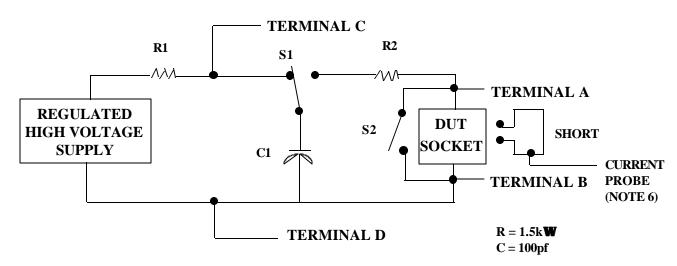
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

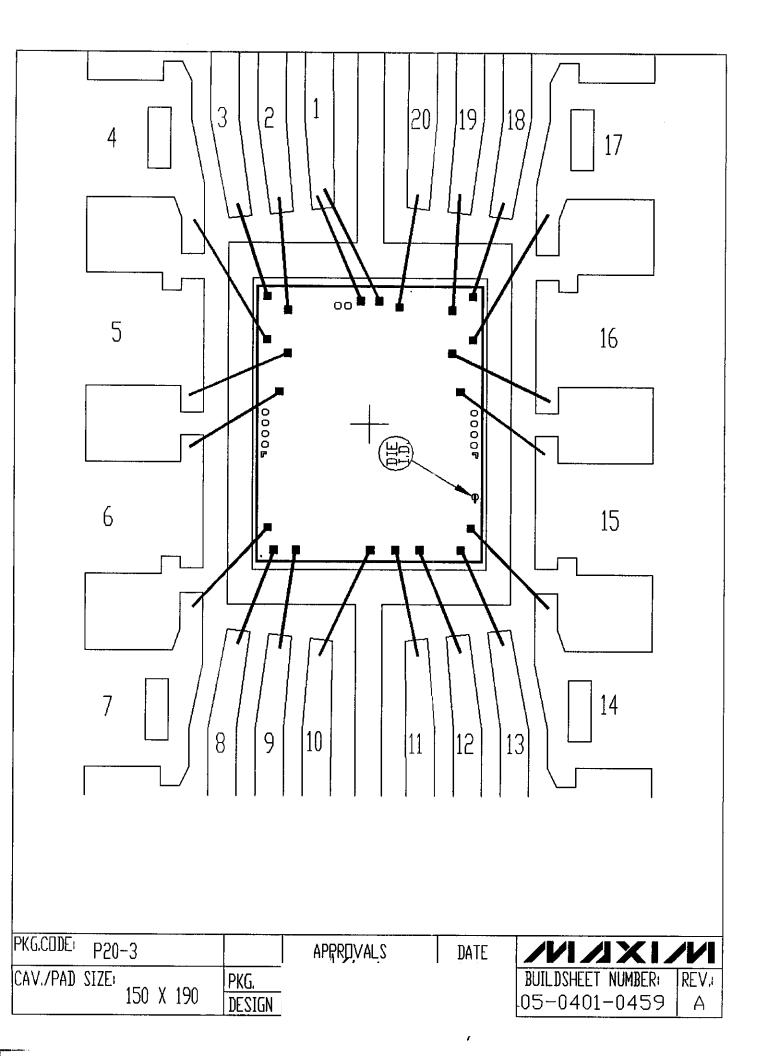
- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

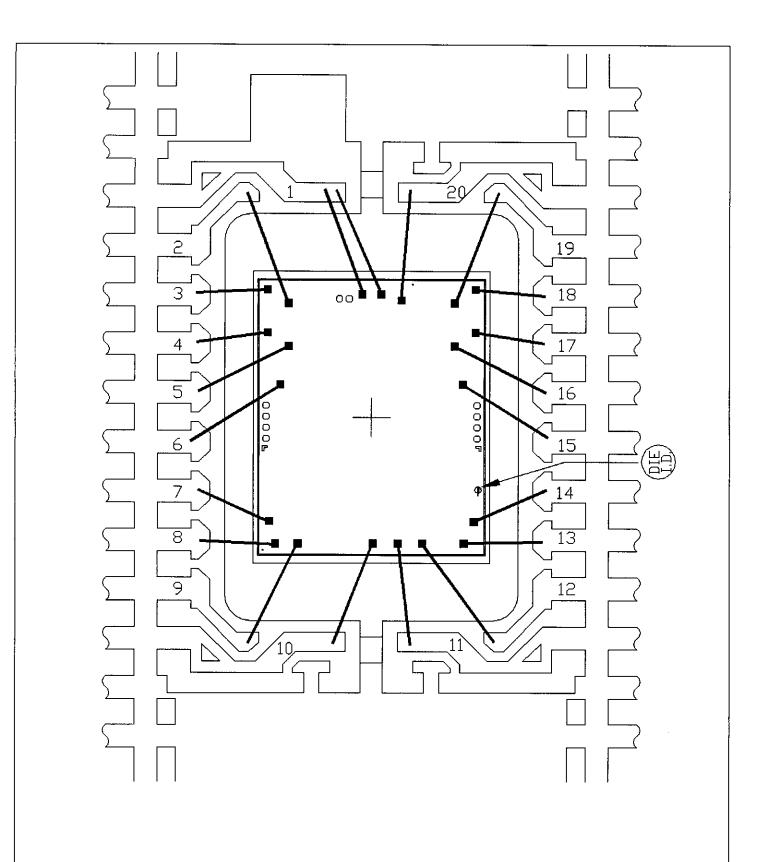
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\lambda_{S1} \), or \(\lambda_{S2} \) or \(\lambda_{S3} \) or \(\lambda_{CC1} \), or \(\lambda_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







PKG.CODE: A20-2		APPROVALS	DATE	NIXI	//
CAV./PAD SIZE:	PKG.			BUILDSHEET NUMBER:	REV.:
154X213	DESIGN			05-0401-0460	Α

