RELIABILITY REPORT

FOR

MAX5180BEEI+

PLASTIC ENCAPSULATED DEVICES

August 1, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX5180BEEI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
.....Attachments
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation

I. Device Description

A. General

The MAX5180 contains two 10-bit, simultaneous-update, current-output digital-to-analog converters (DACs) designed for superior performance in communications systems requiring analog signal reconstruction with low distortion and low-power operation. The MAX5183 provides equal specifications, with on-chip precision resistors for voltage output operation. The devices are designed for 10pV-s glitch operation to minimize unwanted spurious signal components at the output. An on-board 1.2V bandgap circuit provides a well-regulated, low-noise reference that can be disabled for external reference operation. The MAX5180/MAX5183 are designed to provide a high level of signal integrity for the least amount of power dissipation. The DACs operate from a single supply of 2.7V to 3.3V. Additionally, these DACs have three modes of operation: normal, low-power standby, and complete shutdown, which provides the lowest possible power dissipation with 1µA (max) shutdown current. A fast wake-up time (0.5µs) from standby mode to full DAC operation conserves power by activating the DACs only when required. The MAX5180/MAX5183 are packaged in a 28-pin QSOP and are specified for the extended (-40°C to +85°C) temperature range. For lower-resolution, dual 8-bit versions, refer to the MAX5186/MAX5189 data sheet.

II. Manufacturing Information

A. Description/Function:	Dual, 10-Bit, 40MHz, Current/Voltage Simultaneous-Output DACs
B. Process:	TS60
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	October 23, 1999

III. Packaging Information

A. Package Type:	28-pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0505
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	93°C/W
K. Single Layer Theta Jc:	27°C/W
L. Multi Layer Theta Ja:	79.3°C/W
M. Multi Layer Theta Jc:	27°C/W

IV. Die Information

A. Dimensions:	85 X 97 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1 - 0.9 microns / Metal 2 - 0.9 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1 - 0.9 microns / Metal 2 - 0.9 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS60 Process results in a FIT Rate of 0.5 @ 25C and 8.57 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot K6BABQ003A D/C 9951)

The DA70 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX5180BEEI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	K6BCBQ002B, D/C 9947

Note 1: Life Test Data may represent plastic DIP qualification lots.