RELIABILITY REPORT

FOR

MAX5160MEUA

PLASTIC ENCAPSULATED DEVICES

September 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX5160 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5160M linear-taper digital potentiometer performs the same function as a mechanical potentiometer or a variable resistor. It consists of a fixed resistor and a wiper contact with 32 tap points that are digitally controlled by two lines for the MAX5160M.

The MAX5160M is ideal for applications requiring digitally controlled resistors. The resistance value for this part type is 100K Ohms

The MAX5160M is available in a 8-pin uMax package. This device is guaranteed over the extended-industrial temperature range (-40°C to +85°C).

B. Absolute Maximum Ratings

Item	Rating
V_{DD} to GND	-0.3V to +6V
/CS, /INC, U//D to GND	-0.3V to +6V
H, L, W to GND	-0.3V to (VDD +0.3V)
Input and Output Latchup Immunity	±200mA
Maximum Continuous Current into H, L, and W	
MAX516_ _E_ _	±1mA
Operating Temp. Range	-40^0C to $+85^0$C
Storage Temp. Range	-65^0C to 150^0C
Lead Temp. (soldering, 10s)	$+300^0$C
Power Dissipation	
8 Lead uMax	330mW
Derates above +70°C	
8 Leas uMax	4.1mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Power, Dual, 10-Bit Voltage-Output DAC with Serial Interface
B. Process:	SG1.2 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	969
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	September 1999

III. Packaging Information

A. Package Type:	**8 Lead uMax**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-0401-0508
H. Flammability Rating:	Class UL94-V0

IV. Die Information

A. Dimensions:	57 X 34 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5431) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1L).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DA74Z-1Z die type has been found to have all pins able to withstand a transient pulse of ± 2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA and/or ±20V.

Table 1
Reliability Evaluation Test Results
MAX5160MEUA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	140	1
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

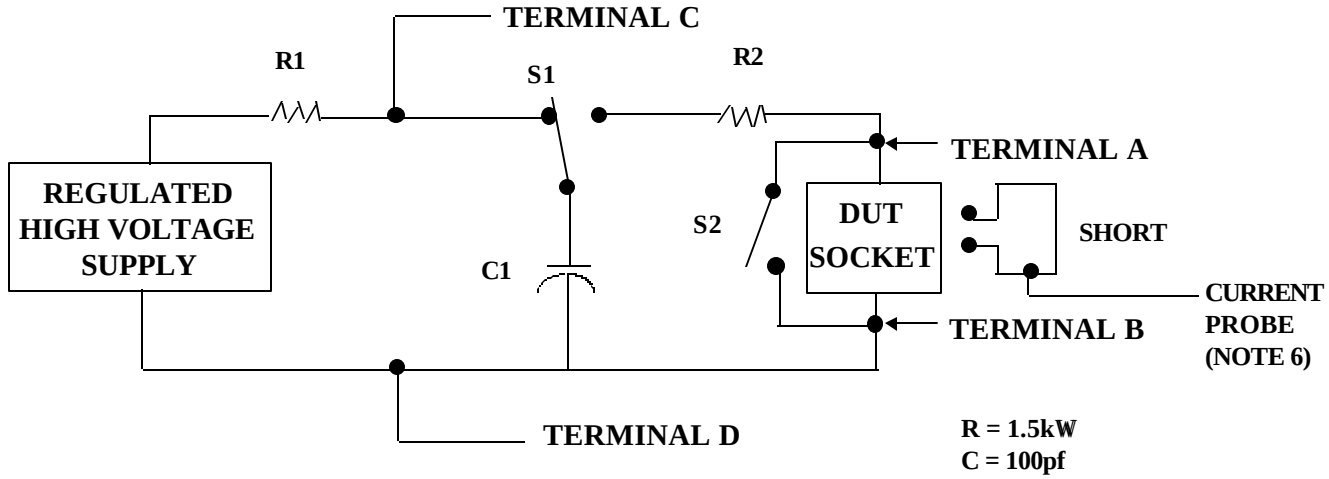
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

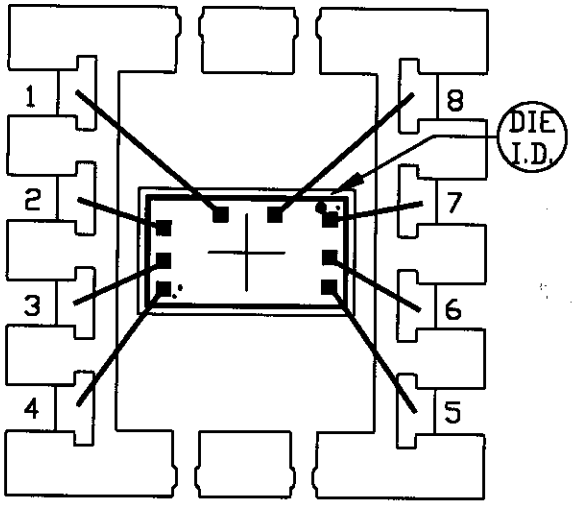
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



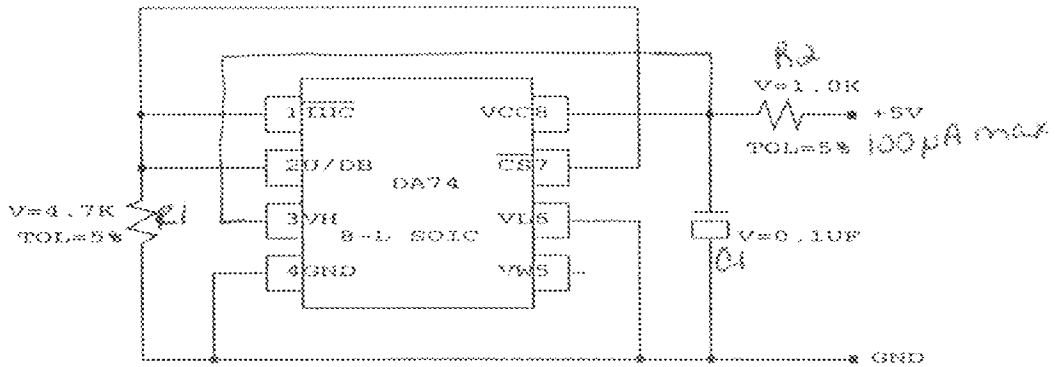
PKG.CODE: U8-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 68X94	PKG. DESIGN		BUILDSHEET NUMBER: 05-0401-0508	REV.: A

Devices which can be burned in with the circuit.

R1

R2

C1



06-5431

MAX5160/1

MAXIM CONFIDENTIAL	CREATED: 00/00/00	BY: JT			ENG2: -
	LAST SAVED: 8-18-1998_9:51		SIZE A	REVISION A 00/00/00	DWG NO. —
BURNIN TEST	PROJECT: DA74				
	DESC.: -		FILE: burnin		SHEET 1 OF 1