RELIABILITY REPORT

FOR

MAX5113GTJ+T / MAX5113GWX+T

PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX5113GTJ+T / MAX5113GWX+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5113 is a 14-bit, 9-channel, current-output digital-to-analog converter (DAC). The device operates from a low +3.0V power supply and provides 14-bit performance without any adjustment. The device’s output ranges are optimized to bias a high power tunable laser source. Each of the 9 channels provides a current source. Channels 1 and 2 provide 10mA current. An internal multiplexer switches the outputs of each channel to one of four external nodes. Channel 3 provides a selectable current of 2mA or 20mA. Channel 4 provides 90mA. Channel 5 provides 180mA. Channel 6 provides a selectable current of -60mA or +300mA. Channel 7 provides 90mA. Channels 8 and 9 provide a selectable current of 15mA or 35mA. Connect DAC outputs in parallel to obtain additional current or to achieve higher resolution. The device contains an internal reference.
An SPI interface drives the device with clock rates of up to 25MHz. An active-high asynchronous CLR input resets DAC codes to zero independent of the serial interface. The device provides a separate power-supply input for driving the interface logic. The MAX5113 is specified over the -40C to +105C temperature range, and is available in 3mm x 3mm, 36-bump WLP and 5mm x 5mm, 32-pin TQFN packages.

II. Manufacturing Information

A. Description/Function:	9-Channel, 14-Bit, Current DAC with SPI Interface	
B. Process:	S45	
C. Fabrication Location:	USA	
D. Assembly Location:	Taiwan, China, Thailand	Japan
E. Date of Initial Production:	June 29, 2012	

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5	36-bump WLP
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Bondwire:	Au (1 mil dia.)	None
E. Mold Material:	Epoxy with silica filler	None
F. Assembly Diagram:	#05-9000-5012	#05-9000-4552
G. Flammability Rating:	Class UL94-V0	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
I. Single Layer Theta Ja:	47°C/W	N/A°C/W
J. Single Layer Theta Jc:	1.7°C/W	N/A°C/W
K. Multi Layer Theta Ja:	29°C/W	38°C/W
L. Multi Layer Theta Jc:	1.7°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	124X120 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
E. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The DB49 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5113GTJ+T / MAX5113GWX+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.