RELIABILITY REPORT

FOR

MAX507xxxG

PLASTIC ENCAPSULATED DEVICES

May 15th, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX507 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX507 is a complete 12-bit, voltage-output digital-to-analog converter (DAC). The DAC output voltage and the reference have the same polarity, allowing single-supply operation. This DAC includes an internal buried-zener reference. Integrating a DAC, voltage-output amplifier, and reference on one monolithic device greatly enhances reliability over multi-chip circuits.

Double-buffered logic inputs interface easily to microprocessors (μPs). Data is transferred into the input register from a 12-bit-wide data bus for 16-bit μPs.

The DAC is specified and tested for both dual- and single-supply operation. Usable supplies range from single +12V to dual ±15V.

On-board gain-setting resistors allow three output-voltage ranges: 0V to +5V and 0V to +10V can be generated when using either single or dual supplies. With dual supplies, ±5V is also available. The output amplifier can drive a 2kΩ load to +10V.

B. Absolute Maximum Ratings

Item	Rating
V_{DD} to AGND	-0.3V, +17V
V_{DD} to DGND	-0.3V, +17V
V_{DD} toV_{SS}	-0.3V, +34V
AGND to DGND	-0.3V, V_{DD}
Digital Input Voltage to GND	-0.3V, V_{DD} +0.3V
V_{OUT} to AGND (Note 1)	V_{SS}, V_{DD}
V_{OUT} to V_{SS} (Note 1)	0v, +34V
V_{OUT} to V_{DD} (Note 1)	-34V, 0V
REFOUT to AGND (Note 1)	-0.3V, V_{DD} +0.3V
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	450mW
Derates above +75°C	6mW/°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin Narrow PDIP	1067mW
24-Pin WSO	941mW
Derates above +70°C	
24-Pin Narrow PDIP	13.3mW/°C
24-Pin WSO	11.8mW/°C

II. Manufacturing Information

A. Description/Function:	Voltage-Output, 12-Bit DAC with Internal Reference
B. Process:	SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	650
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	January, 1992

III. Packaging Information

A. Package Type:	**24-Lead Narrow PDIP**	**24-Lead WSO**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0401-0123	# 05-0401-0118
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	142x140 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Reliability Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 577 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 1.88 \times 10^{-9}$ $\lambda = 1.88$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-2788) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA21 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

MAX507xxxG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		577	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	WSO PDIP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

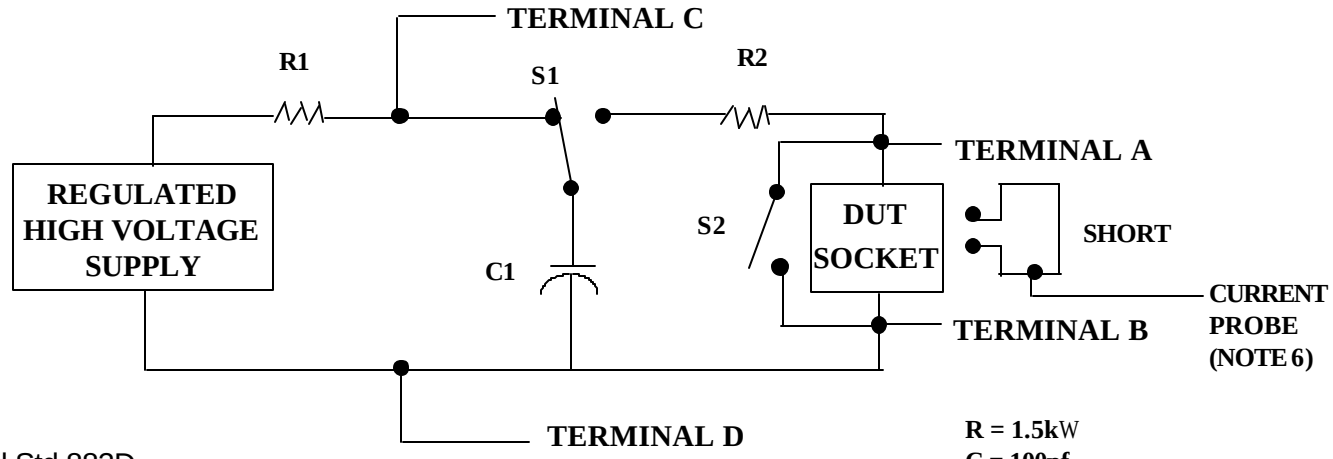
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

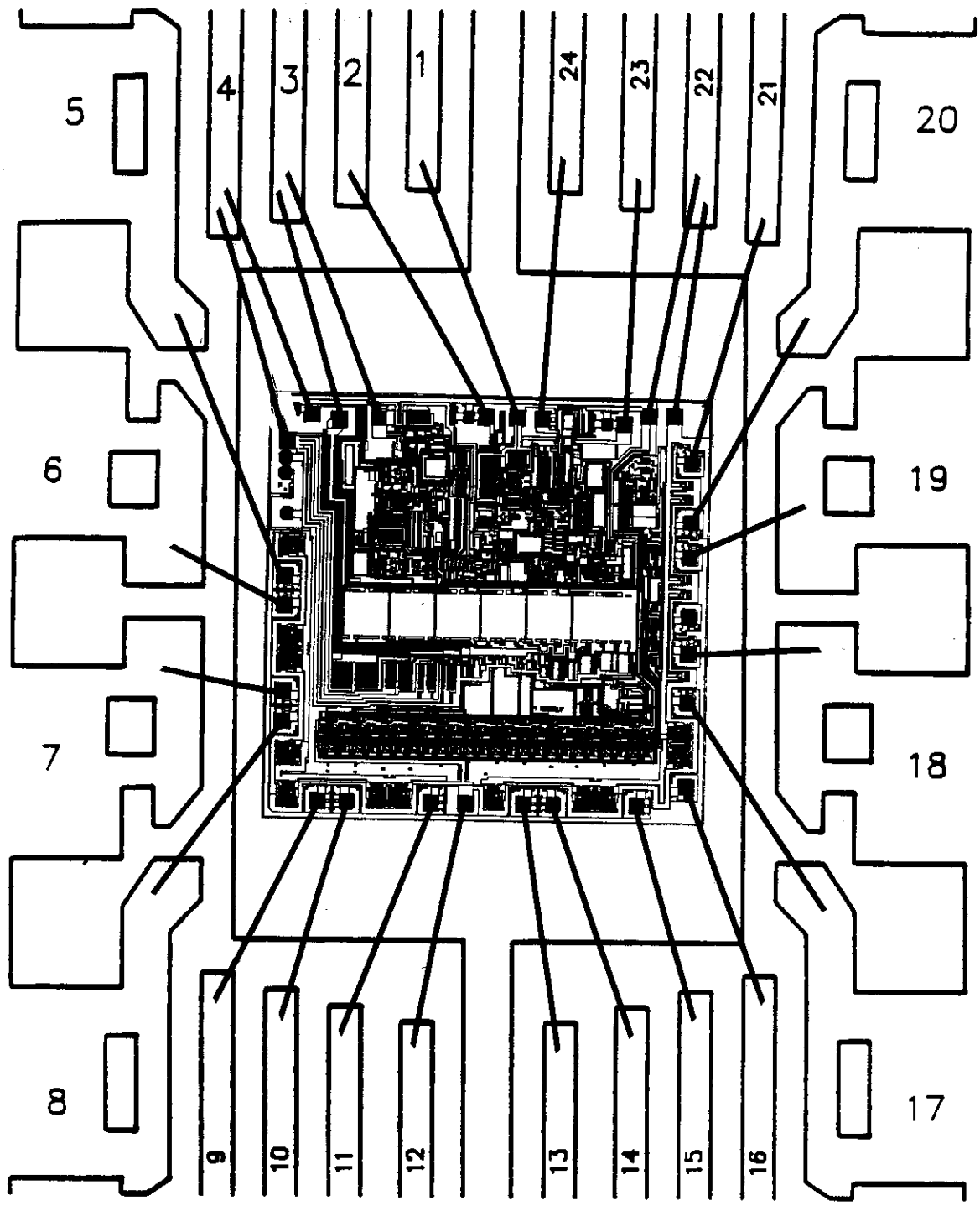
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

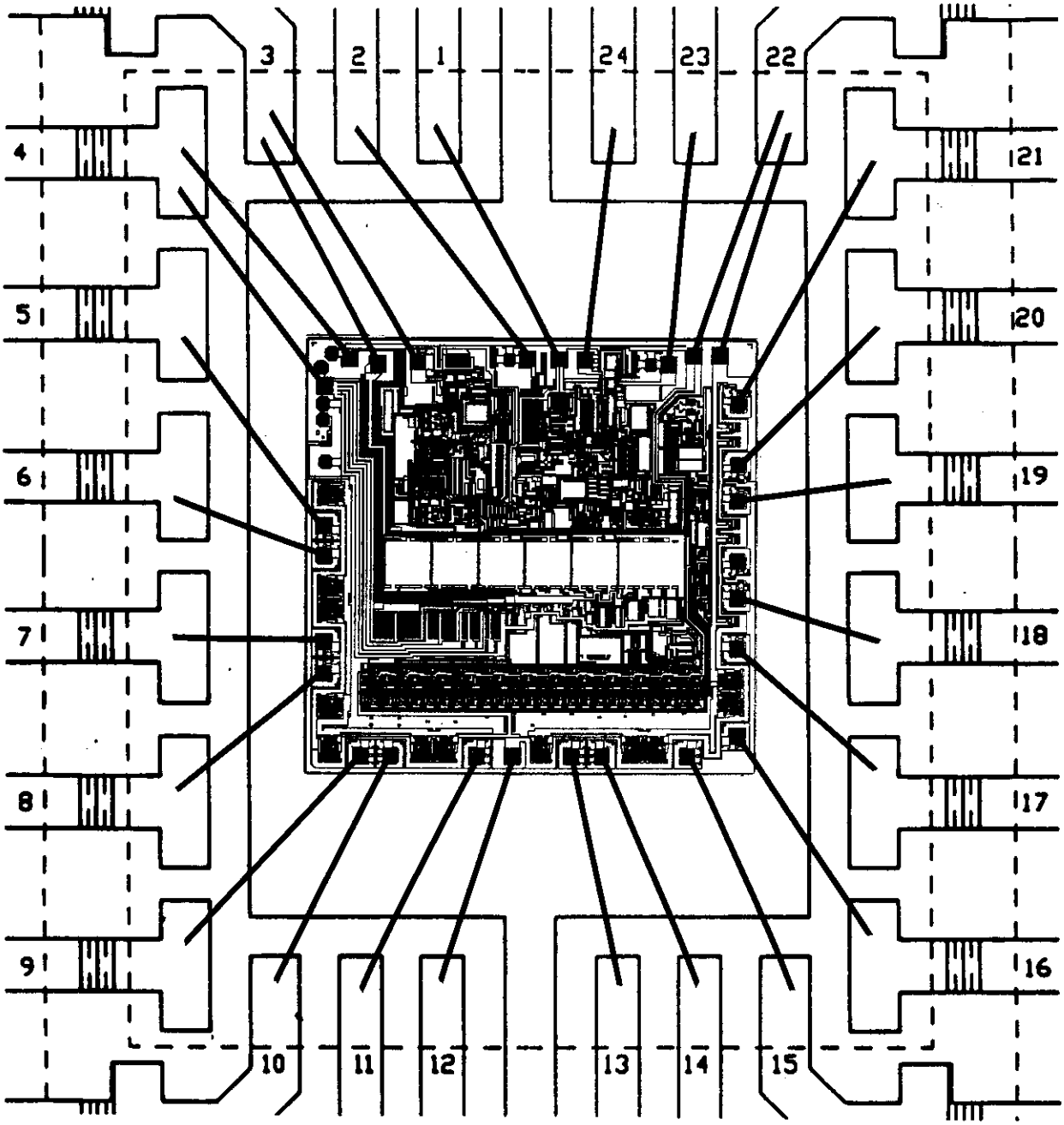
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



MAXIM	APPROVALS	DATE	DIE TYPE: DA21Y
	PKG.		SIZE (MILS): 142 X 140
PKG. TYPE: 24L Nar. PDip	DESIGN		STEP: 7
PKG. CODE: N24-3	D/A PREFORM STOCK NUMBER:		PRODUCT NAMES
CAV/PAD SIZE: 160 X 210	n/a		1. MX7245
APPROVED:	LEADFRAME MATERIAL:		2. MAX507
COMM. [X] 883/HR [ ]	Spot Silver on Copper		3.
SCALE: 20:1 0 1	SPECIAL NO:		4.
BUILDSHEET NUMBER: 05-0401-0123 REV. D			5.
			6.

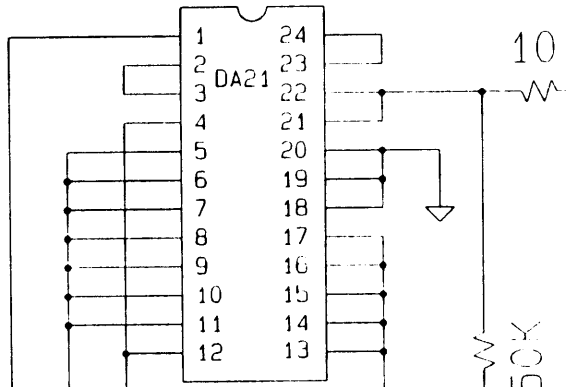


MAXIM	APPROVALS	DATE	DIE TYPE: DA21Y
	PKG.		SIZE (MILS): 142 X 140
PKG. TYPE: 24L Wide SOIC	DESIGN		STEP: 7
PKG. CODE: SW24-2	D/A PREFORM STOCK NUMBER:		PRODUCT NAMES
CAV/PAD SIZE: 170 X 220	N/A		1. MX7245
APPROVED:	LEADFRAME MATERIAL:		2. MAX507
COMM. [X] 883/HR [ ]	Spot Ag on Copper		3.
SCALE: 20:1 0 1	SPECIAL NOTES:		4.
BUILDSHEET NUMBER: 05-0401-0118 REV. C			5.
			6.

ONCE PER SOCKET

Top View

24 SKINNY DIP
MX7245 or MAX507



10 — VDD=15V (I=12mA MAX)

50K

1K — CLK1

10 — VSS=-15V (I=5mA MAX)

$P_{d\,(max)} = 255mW$

$T_{max} = 125^{\circ}C$

RESISTORS ARE 1/4W, 1%
BYPASS VDD AND VSS WITH 0.1uF EVERY 10 DEVICES

Steady state life test is per MIL-STD-883 Method 1005.

Burn-in is per MIL-STD-883 Method 1015. COND. _____

ONCE PER BOARD

NOTE 4

+5V	I=	
-5V	I=	
+10V	I=	
-10V	I=	
+15V	I=	
-15V	I=	
+20V	I=	
-20V	I=	
CLK 1	FREQ =	AMP =
CLK 2	FREQ =	AMP =
CLK 3	FREQ =	AMP =
CLK 4	FREQ =	AMP =
GND		

NOTES:
1. **TEMPERATURE: +125 DEGREES C OR EQUIVALENT**
2. **TIME: 160 HOURS MIN. OR EQUIVALENT**
3. **PACKAGE TYPE:**
4. **MAX. SUPPLY CURRENT PER DEVICE:**
5. **C = C = 0.1 uf ± 20%**
6. **R_1**
7. **BURN-IN BOARD MATERIAL & ALL COMPONENTS MUST WITHSTAND + 150° C CONTINUOUS OPERATION.**

SPEC. NO. 06-2788 REV. #	MAXIM BURN-IN SCHEMATIC
DATE:	(DA21) MX7245, MAX507
DRAWN BY:	
APPROVED BY DATE	SCALE: