RELIABILITY REPORT

FOR

MAX5024xASA

PLASTIC ENCAPSULATED DEVICES

August 24, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX5024 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5024 high-voltage linear regulator operates from a +6.5V to +65V input voltage and delivers up to 150mA of output current. This devices consumes only $60\mu\text{A}$ of quiescent current with no load and withstands a -60V reverse battery voltage at the input. The MAX5024 includes an active-low internal microprocessor (μP) reset circuit that asserts when the regulator output drops below the preset output voltage threshold by 7.5% or 12.5%, depending on the device selected. The device is available with a fixed +3.3V or +5V output. The device is short-circuit protected and includes thermal shutdown.

In addition to an enable input to turn the regulator on or off, the MAX5024 includes a HOLD-bar input that allows for the implementation of a self-holding circuit without requiring external components. Setting HOLD-bar low after enabling the regulator forces the regulator to remain on, even if EN is subsequently set low. Releasing HOLD-bar shuts down the regulator.

The MAX5024 includes a SET input that, when connected to ground, selects a preset output voltage of +3.3V (MAX5024S/MAX5024T) or +5V (MAX5024L/MAX5024M). Set the adjustable output voltage by connecting SET to the regulator's output through a resistive-divider network.

The MAX5024 operates over the automotive temperature range (-40°C to +125°C), and is available in a thermally enhanced, surface-mount 8-pin SO package.

Rating

B. Absolute Maximum Ratings

Item

	
IN to GND	-60V to +70V
EN to GND	-0.3V to (VIN + 0.3V)
HOLD to GND	-0.3V to (VOUT + 0.3V)
SET, WDI, OUT to GND	-0.3V to +13.2V
RESET to GND (Open Drain)	-0.3V to +13.2V
Short-Circuit Duration	Continuous
Maximum Current to Any Pin (Except IN, OUT)	±20mA
Thermal Resistance:	
(Theta JA)	52°C/W
(Theta JC)	2°C/W
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70C)	
8-PIN SO	1538mW
Derates above +70°C	
8PIN SO	19.2mW/°C

II. Manufacturing Information

A. Description/Function: 65V, Low-Quiescent-Current, High-Voltage Linear Regulators with µP Reset and Watchdog Timer

B. Process: BCD80

C. Number of Device Transistors: 1382

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines

F. Date of Initial Production: October, 2002

III. Packaging Information

A. Package Type: 8-Pin NSO

B. Lead Frame: Copper

C. Lead Finish: Solder Plate or 100% Matte Tin

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-1301-0040

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

A. Dimensions: 85 X 112 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}}_{} = \underbrace{\frac{1.83}{192 \times 4389 \times 43 \times 2}}_{} \text{(Chi square value for MTTF upper limit)}$$

$$\underbrace{\frac{1}{\text{Temperature Acceleration factor assuming an activation energy of } 0.8eV}_{}$$

$$\lambda = 25.57 \times 10^{-9}$$

 λ = 25.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5892) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the BCD80 Process results in a FIT rate of 0.38 @ 25°C and 6.59 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The NP33-1 die type has been found to have all pins able to withstand a transient pulse of ± 2000 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX5024xASA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		43	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

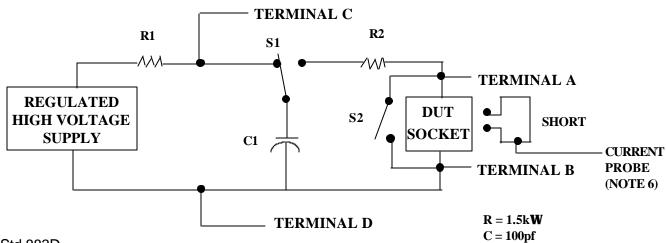
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

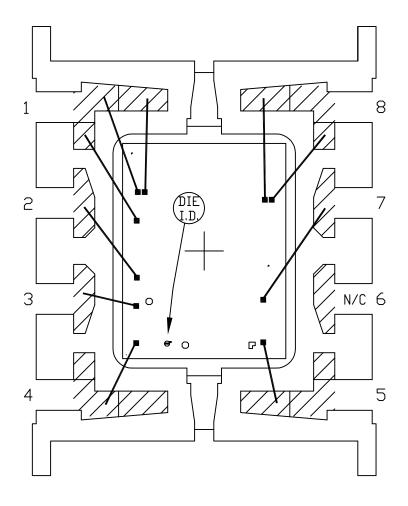
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\lambda_{S1} \), or \(\lambda_{S2} \) or \(\lambda_{S3} \) or \(\lambda_{C1} \), or \(\lambda_{C2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8

EXPOSED PAD PKG.





PKG. CODE: S8E-14		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
95×122	DESIGN			05-1301-0040	C

