RELIABILITY REPORT

FOR

MAX4948ETG+

PLASTIC ENCAPSULATED DEVICES

May 11, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX4948ETG+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4947/MAX4948 analog switches operate from a single +1.8V to +5.5V supply. These switches feature a low 30pF (typ) capacitance for high-speed data switching applications. The MAX4947 is a triple double-pole/double-throw (DPDT) switch, and the MAX4748 is a hex single-pole/double-throw (SPDT) switch with one control logic input. The MAX4947 has three logic inputs to control the switches in pairs. The MAX4948 has one logic input and an enable input (active-low EN) to disable the switches. The MAX4947/MAX4948 are available in small 24-pin (4mm x 4mm) TQFN and 25-bump (2.5mm x 2.5mm) chip-scale packages (UCSP(tm)).-

II. Manufacturing Information

A. Description/Function:	Hex SPDT Data Switch
B. Process:	VS50
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	China, Thailand, Malaysia, Philippines
F. Date of Initial Production:	January 20, 2007

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2577
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2.7°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	100X100 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.50um
F. Minimum Metal Spacing:	0.50um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

B. E.S.D. and Latch-Up Testing (lot LCGYAQ001C, 0637)

The AJ03-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4948ETG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	LCGYAQ001C, D/C 0637

Note 1: Life Test Data may represent plastic DIP qualification lots.