RELIABILITY REPORT

FOR

MAX4906FELB

PLASTIC ENCAPSULATED DEVICES

July 10, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Conclusion

The MAX4906F successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4906F analog switches combine the low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications. This device is designed for USB 2.0 high-speed applications at 480Mbps. These switches will also handle all the requirements for USB low- and full-speed signaling.

The MAX4906F feature two single-pole/double- throw (SPDT) switches. This device is fully specified to operate from a single +3.0V to +3.6V power supply and are protected against a +5.5V short to COM1 and COM2. This feature makes them fully compliant with the USB 2.0 specification of +5.5V fault protection. This device features a low threshold voltage and a +1.4V V_{IH}, permitting them to be used with low-voltage logic. The MAX4906F operatse at 300µA (max) quiescent current and feature a shutdown input to reduce the quiescent current to less than 2µA (max).

The MAX4906F is available in space-saving, 2mm x 2mm µDFN packages and operates over a -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
Voltages Referenced to GND	
V+	-0.3V to +4V
IN, SHDN, SHDN/EN (Note 1)	-0.3V to (V+ + 0.3V)
COM_, NO_, NC_	-0.5V to +5.5V
Continuous Current (COM_ to NO_/NC_)	±120mA
Peak Current, (COM_ to NO_/NC_) (pulsed at 1ms 10% duty cycle)	±240mA
Continuous Power Dissipation (TA = +70°C)	
10-Pin TDFN (derate 18.5mW/°C above +70°C)	1482mW
10-Pin µDFN (derate 5.3mW/°C above +70°C)	423.7mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on IN, SHDN or SHDN/EN exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating

II. Manufacturing Information

A. Description/Function:	High-/Full-Speed USB 2.0 Switches
B. Process:	S4
C. Number of Device Transistors:	2556
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand or Hong Kong
F. Date of Initial Production:	December, 2005

III. Packaging Information

	10-Pin TDFN (3x3)	**10-Pin µDFN**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Gold Plate
D. Die Attach:	Silver-Filled Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1774	# 05-9000-1776
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	55 x 41 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1, Metal2 & Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1, Metal2 & Metal3 = 0.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 11.95 \times 10^{-9}$

λ = 11.95 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6501) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S4 Process results in a FIT Rate of 0.56 @ 25C and 9.60 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AS54 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4906FEBL

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uDFN TQFN	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

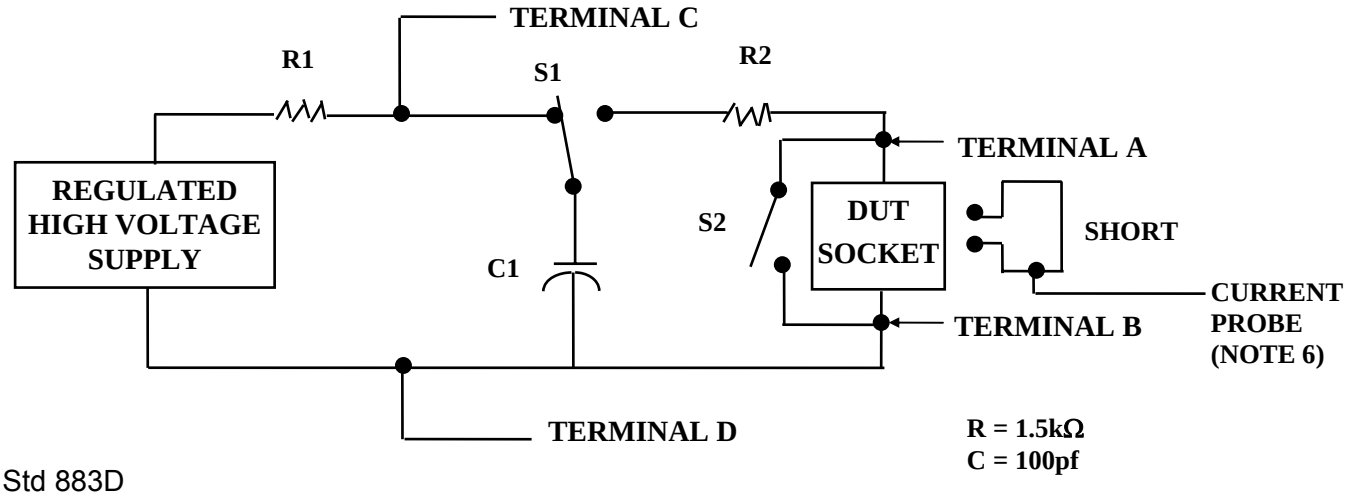
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

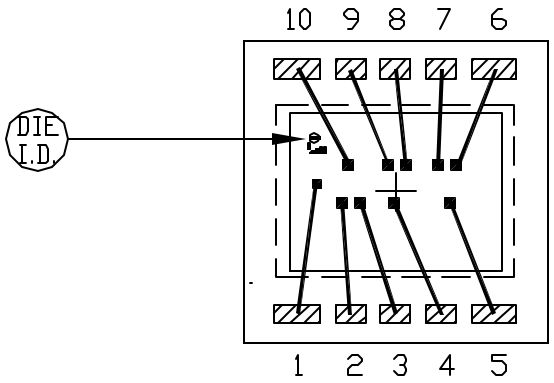
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

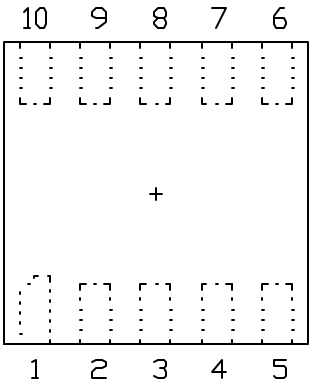


Mil Std 883D
Method 3015.7
Notice 8

2x2x0.8mm uDFN



TOP VIEW



TOP VIEW OF BOTTOM LEADS

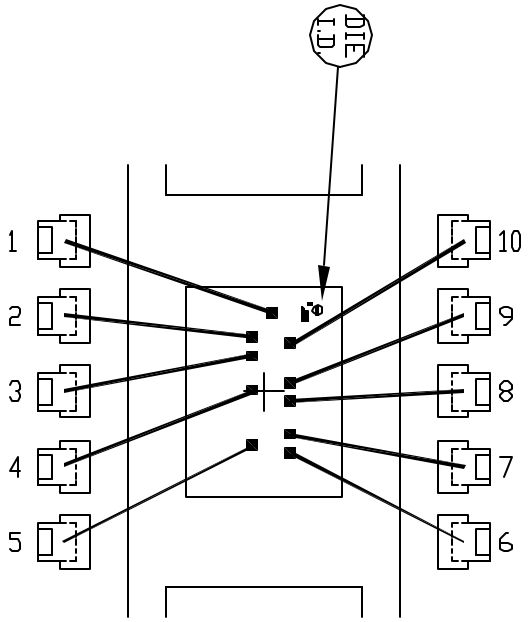
BONDABLE AREA

MAX. DIE PLACEMENT AREA

USE NON-CONDUCTIVE EPOXY

PKG. CODE: L1022-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: – –	PKG.			BOND DIAGRAM #: 05-9000-1776	REV: B
	DESIGN				

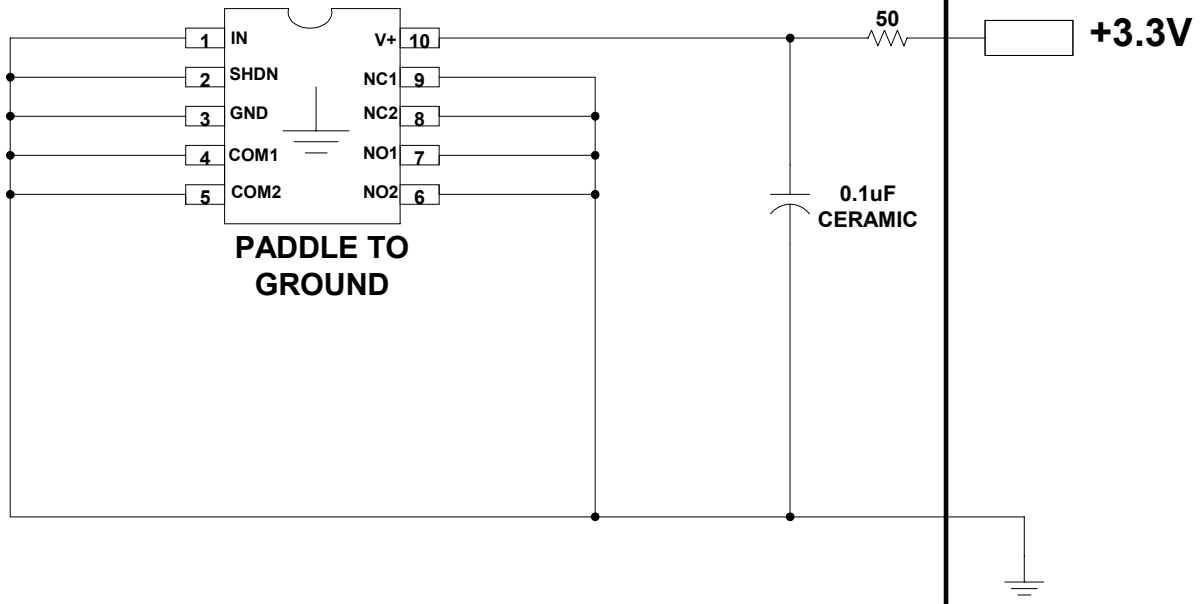
3x3x0.8 MM TDFN PKG. EXPOSED PAD PKG.



PKG. CODE: T1033-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71x102	PKG.			BOND DIAGRAM #: 05-9000-1774	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICE: MAX4906 (AS54)
PACKAGE: 10-TDFN 3x3
MAX EXPECTED CURRENT: 0.5mA, TYPICAL: 0.25mA

NOTE: ALL RESISTORS ARE 1/4W.