RELIABILITY REPORT

FOR

MAX4901EBL+

CHIP SCALE PACKAGE

October 16, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX4901EBL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX4901-MAX4905 switches feature negative signal capability that allows signals below ground to pass through without distortion. The MAX4901/MAX4902 are a dual SPST (single-pole/single-throw) and the MAX4903/MAX4904/MAX4905 are a single SPDT (single-pole/double-throw) configuration. These analog switches operate from a single +1.8V to +5.5V supply and have low 0.6 on-resistance, making them ideal for switching audio signals. The MAX4905 includes a comparator that can be used for headphone detection or mute/send key function. The MAX4902/MAX4904/MAX4905 have internal shunt resistors to automatically discharge any capacitance at the NO_ and NC connection points. This reduces click-and-pop sounds that occur when switching audio signals between pre-charged points. A break-before-make feature and auto-discharge also help to reduce popping. These SPST and SPDT switches are available in space-saving 8-pin TDFN and 9-bump UCSP(tm) packages and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Low-R_{ON}, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability
B. Process:	0.6um CMOS
C. Number of Device Transistors:	511
D. Fabrication Location:	Sunnyvale
E. Assembly Location:	Dallas, Casio
F. Date of Initial Production:	October 22, 2005

III. Packaging Information

A. Package Type:	9-pin UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-1889
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	N/A
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	62 X 62 mils
B. Passivation:	Oxide/Nitride
C. Interconnect:	Al/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.6 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.6 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 21.5 \times 10^{-9}$

$\lambda = 21.5$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the C6 Process results in a FIT Rate of 0.82 @ 25C and 14.21 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AS60 die type has been found to have all pins able to withstand a HBM transient pulse of 2500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of 250 mA.

Table 1
Reliability Evaluation Test Results

MAX4901EBL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 125C Biased Time = 192 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	160	0
Mechanical Stress (Note 2 & 3)				
Temperature Cycle	-40ºC/125ºC 1000 Cycles (Note 3)	DC Parameters & functionality	160	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: Ramp rate 11ºC/minute, dwell=15 minutes, One cycle/hour.