RELIABILITY REPORT

FOR

MAX4820ExP

PLASTIC ENCAPSULATED DEVICES

April 6, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4820 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4820 8-channel relay drivers offer built-in kickback protection and drive +3.3V/+5V nonlatching or dual-coil-latching relays. This device is especially useful when driving +3V relays. Each independent open-drain output features a 2Ω on-resistance and is guaranteed to sink 70mA (min) of load current. Both devices consume less than 50µA (max) quiescent current and have 1µA output off-leakage current.

The MAX4820 features an SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. Input data is shifted into an 8-bit shift register and latched to the outputs when CS-bar transitions from low to high. Each data bit in the shift register corresponds to a specific output, allowing independent control of all outputs. The device features separate set and reset functions that allow the user to turn on or turn off all outputs simultaneously with a single control line. Built-in hysteresis (Schmidt trigger) on all digital inputs allows these devices to be used with slow rising and falling signals, such as those from optocouplers or RC power-up initialization circuits. The MAX4820 is available in 20-pin TSSOP and space-saving 20-pin thin QFN packages.

B. Absolute Maximum Ratings

Item	Rating
(All voltages referenced to GND.)	
VCC, COM	-0.3V to +6.0V
OUT_	-0.3V to (VCOM + 0.3V)
CS, SCLK, DIN, SET, RESET, A0, A1, A2, LVL	-0.3V to +6.0V
DOUT	-0.3V to (VCC + 0.3V)
Continuous OUT_ Current (all outputs turned on)	150mA
Continuous OUT_ Current (single output turned on)	300mA
Continuous Power Dissipation (TA = +70°C)	
20-Pin TSSOP	1739mW
20-Pin QFN	1350mW
Derates above +70°C	
20-Pin TSSOP	21.7mW/°C
20-QFN	16.9mW/°C
?JA	
20-Pin TSSOP	46°C/W
20-QFN	59.3°C/W

II. Manufacturing Information

A. Description/Function:	+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface
B. Process:	B8
C. Number of Device Transistors:	1301
D. Fabrication Location:	California, USA
E. Assembly Location:	Hong Kong, Philippines, Korea or Thailand
F. Date of Initial Production:	January, 2003

III. Packaging Information

A. Package Type:	**20-Lead TSSOP**	**20-Lead QFN (4x4)**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0318	# 05-9000-0315
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	70 x 70 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6101) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH98 die type has been found to have all pins able to withstand a transient pulse of 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4820ExP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP QFN	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

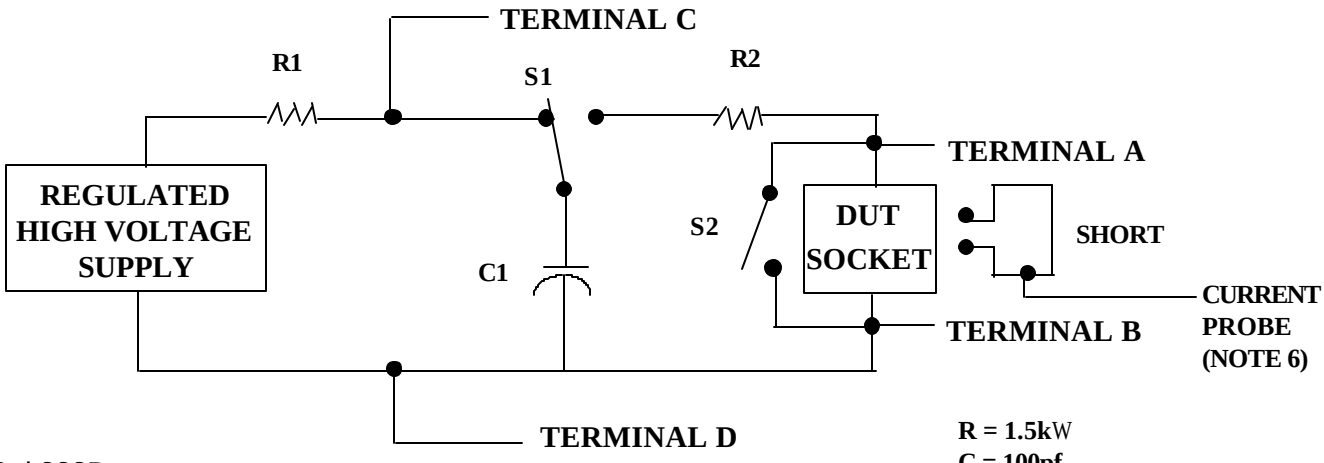
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

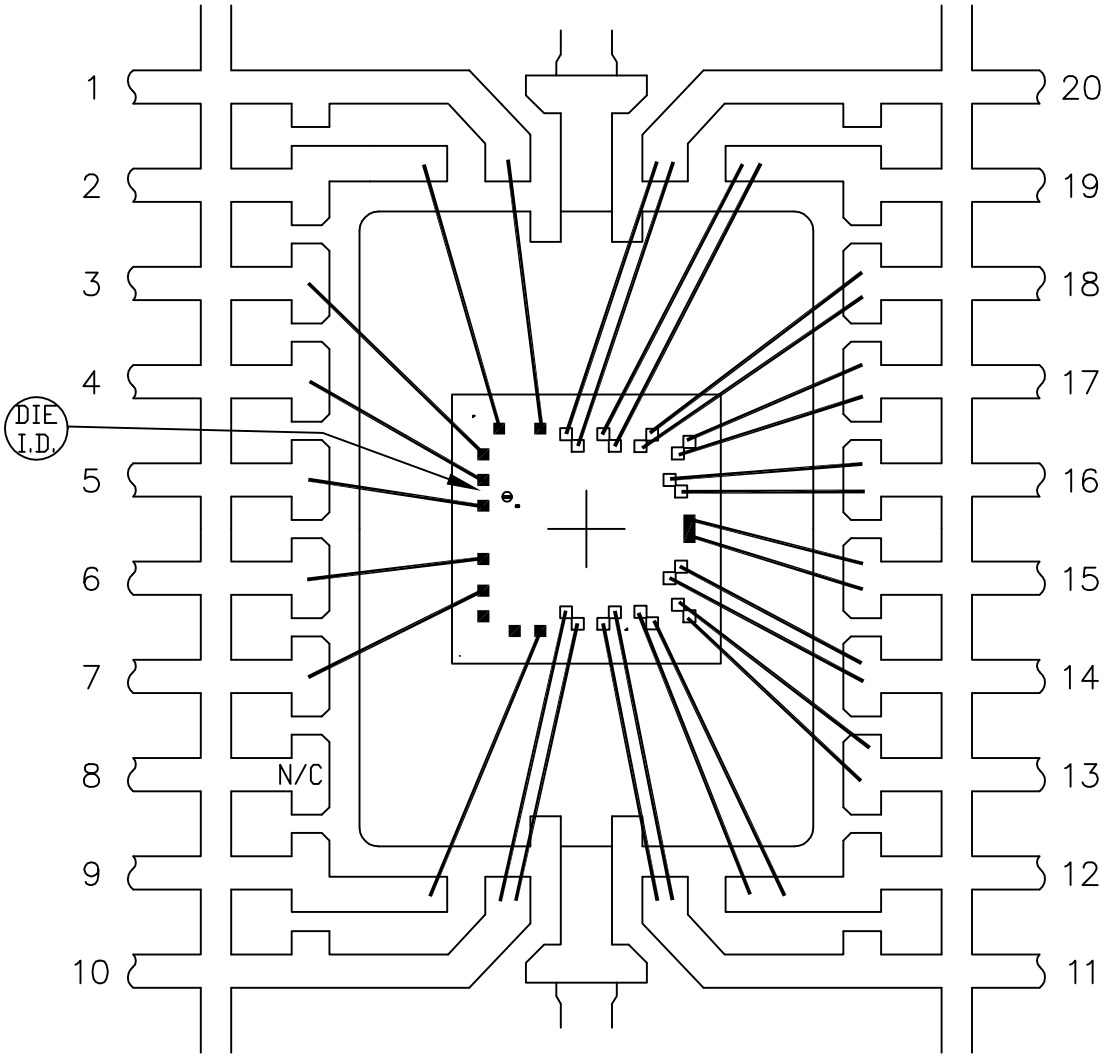
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



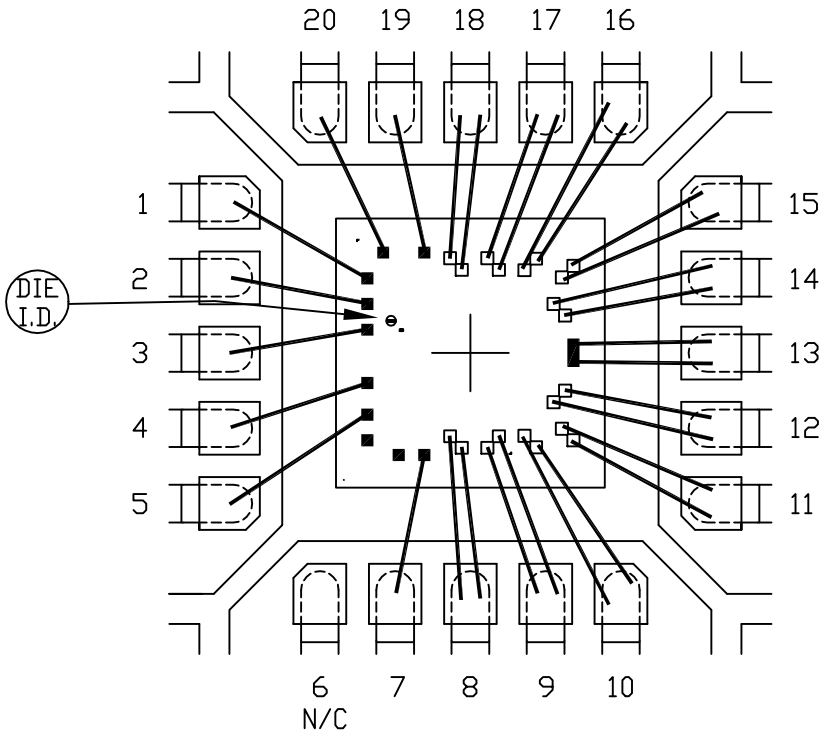
Mil Std 883D
Method 3015.7
Notice 8

EXPOSED PAD PKG.

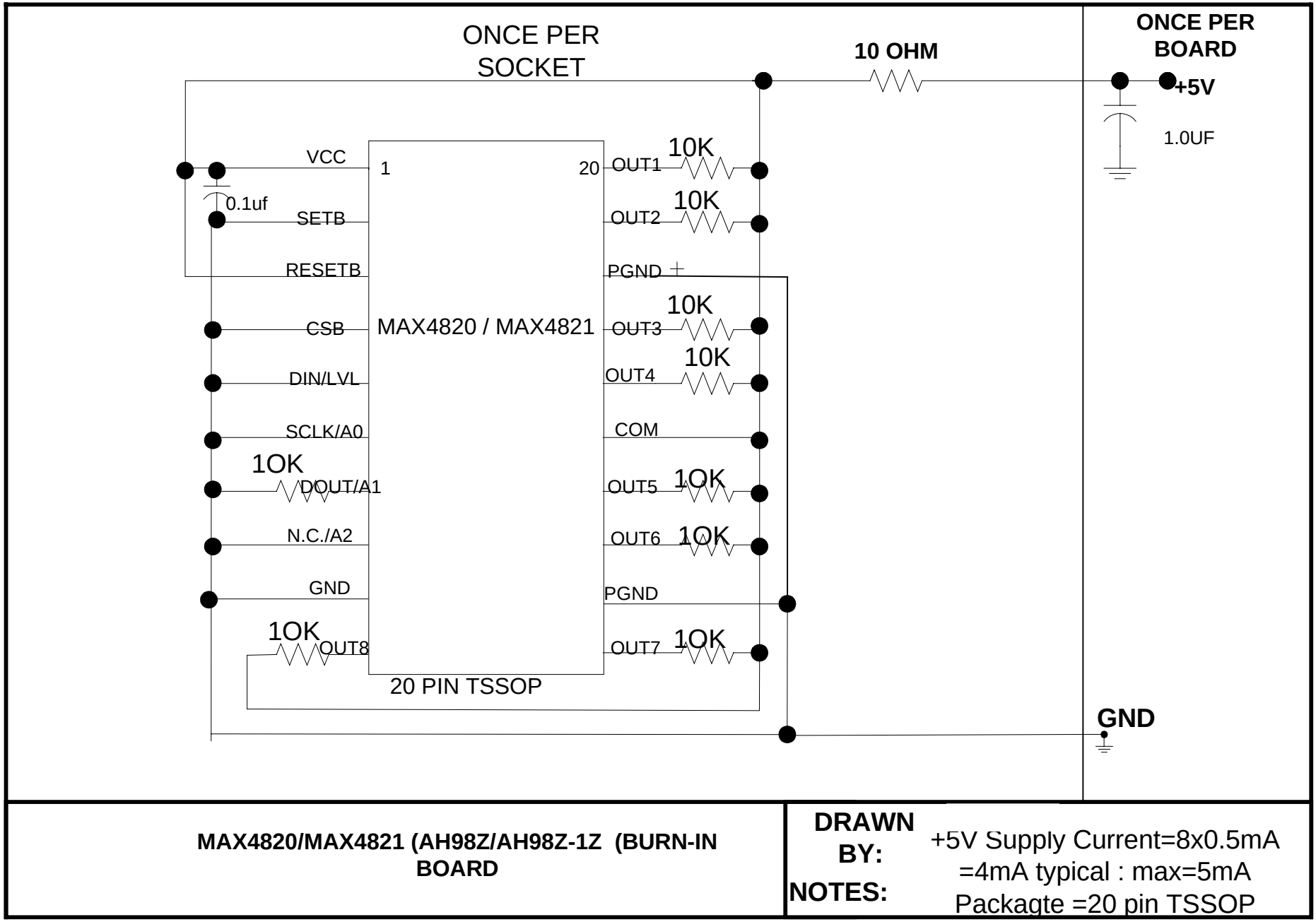


PKG. CODE: U20E-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x165	PKG.			BOND DIAGRAM #: 05-9000-0315	REV: A
	DESIGN				

4x4x0.80mm QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T2044-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 98x98	PKG.			BOND DIAGRAM #: 05-9000-0318	REV: B
	DESIGN				



MAX4820/MAX4821 (AH98Z/AH98Z-1Z (BURN-IN BOARD	**DRAWN BY:**
	NOTES: +5V Supply Current=8x0.5mA =4mA typical : max=5mA Packagte =20 pin TSSOP