RELIABILITY REPORT

FOR

MAX4762Exx

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

April 4, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Reviewed by

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Conclusion

The MAX4762 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4762 dual SPDT (single-pole/double-throw) switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single +1.8V to +5.5V supply and have low 0.6Ω on-resistance, making them ideal for switching audio signals.

These SPDT switches are available in space-saving µMAX, TDFN, and UCSP™ packages and operate over the -40°C to +85°C extended temperature range.

B. Absolute Maximum Ratings

Item	Rating
(All voltages referenced to GND.)	
VCC, IN_, CMP-	-0.3V to +6.0V
COM_, NO_, NC_	(VCC - 6V) to (VCC + 0.3V)
CMPO	-0.3V to (VCC + 0.3V)
Closed-Switch Continuous Current COM_, NO_, NC_	±150mA
Open-Switch Continuous Current NO_, NC_(MAX4764/MAX4765)	±30mA
Peak Current COM_, NO_, NC_ (pulsed at 1ms, 50% duty cycle)	±300mA
Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle)	±400mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C
Continuous Power Dissipation	
10-Lead µMAX	444mW
10-Lead Thin DFN	1951mW
12-Bump UCSP	519mW
Derates above +70°C	
10-Lead µMAX	5.6mW/°C
10-Lead Thin DFN	24.4mW/°C
12-Bump UCSP	6.5mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Voltage, Dual SPDT, Audio Clickless Switches with Negative Rail Capability
B. Process:	S6 (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors:	768
D. Fabrication Location:	Japan, USA
E. Assembly Location:	Philippines, China, Thailand, USA, Taiwan
F. Date of Initial Production:	January 24, 2004

III. Packaging Information

A. Package Type:	**10-Lead uMAX**	**10-Lead Thin DFN**	**12-Bump UCSP**
B. Lead Frame:	Copper	Copper	N/A
C. Lead Finish:	Solder Plate	Solder Plate	N/A
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy	N/A
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-9000-0961	# 05-9000-0962	# 05-9000-0965
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	83 x 62 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$

$\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6306) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AS37 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4762Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX TDFN UCSP	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	uMAX TDFN UCSP	77 77 N/A	0 0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010 (Note 3)	DC Parameters & functionality	TSSOP UCSP	77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

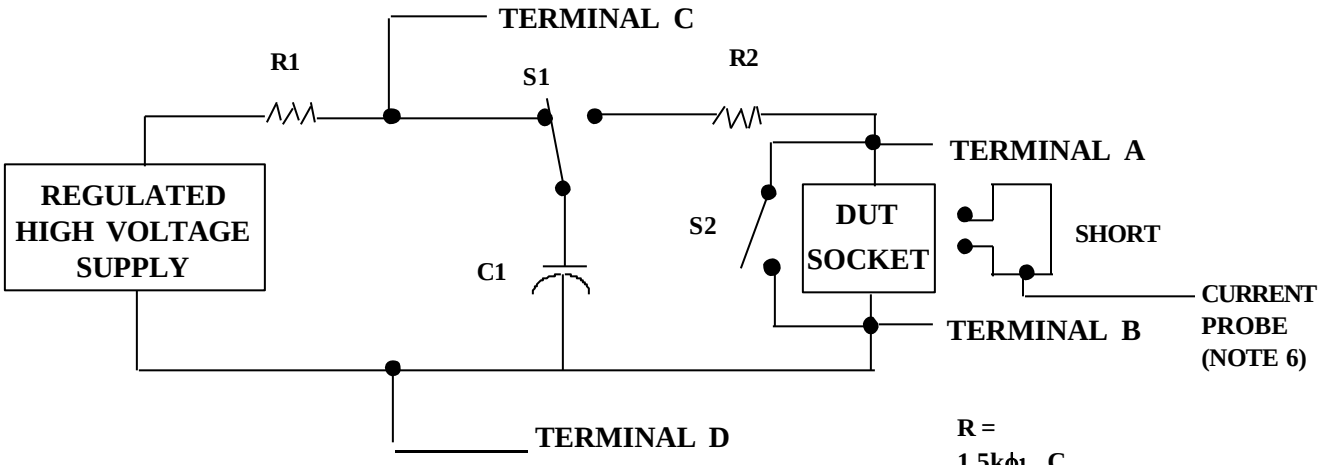
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

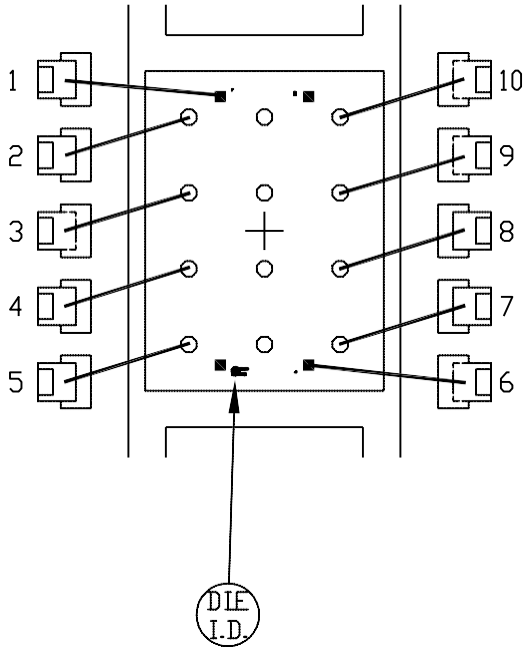
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

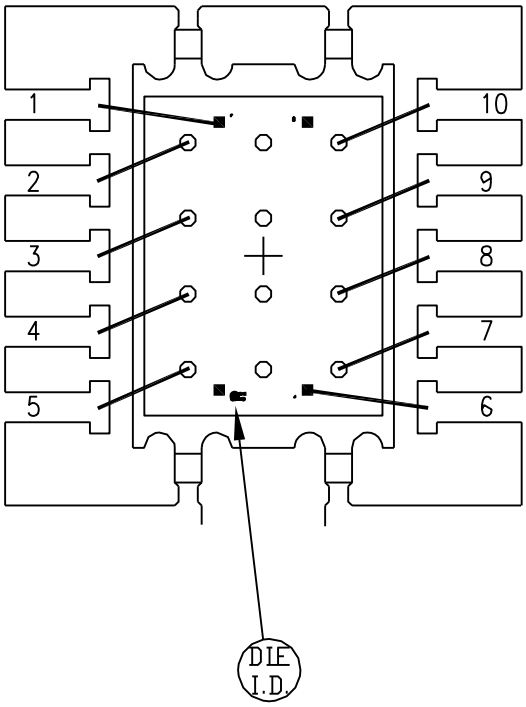


Mil Std 883D
Method 3015.7
Notice 8

3x3x0.8 MM TDFN PKG. EXPOSED PAD PKG.

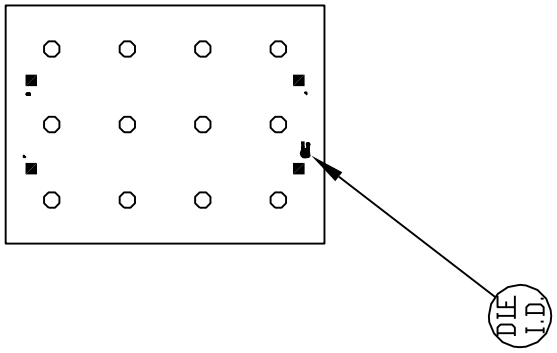


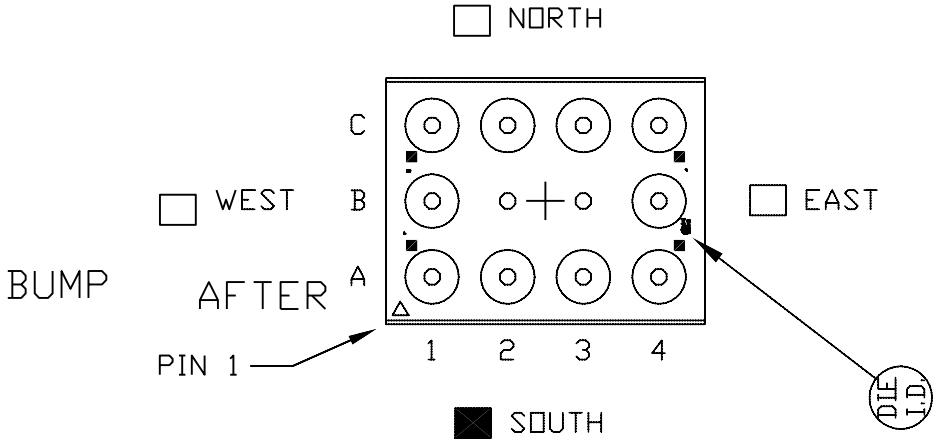
PKG. CODE: T1033-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71×102	PKG.			BOND DIAGRAM #: 05-9000-0962	REV: A
	DESIGN				



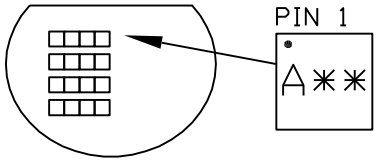
PKG. CODE: U10-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG.			BOND DIAGRAM #: 05-9000-0961	REV: A
	DESIGN				

ORIGINAL CHIP





SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.

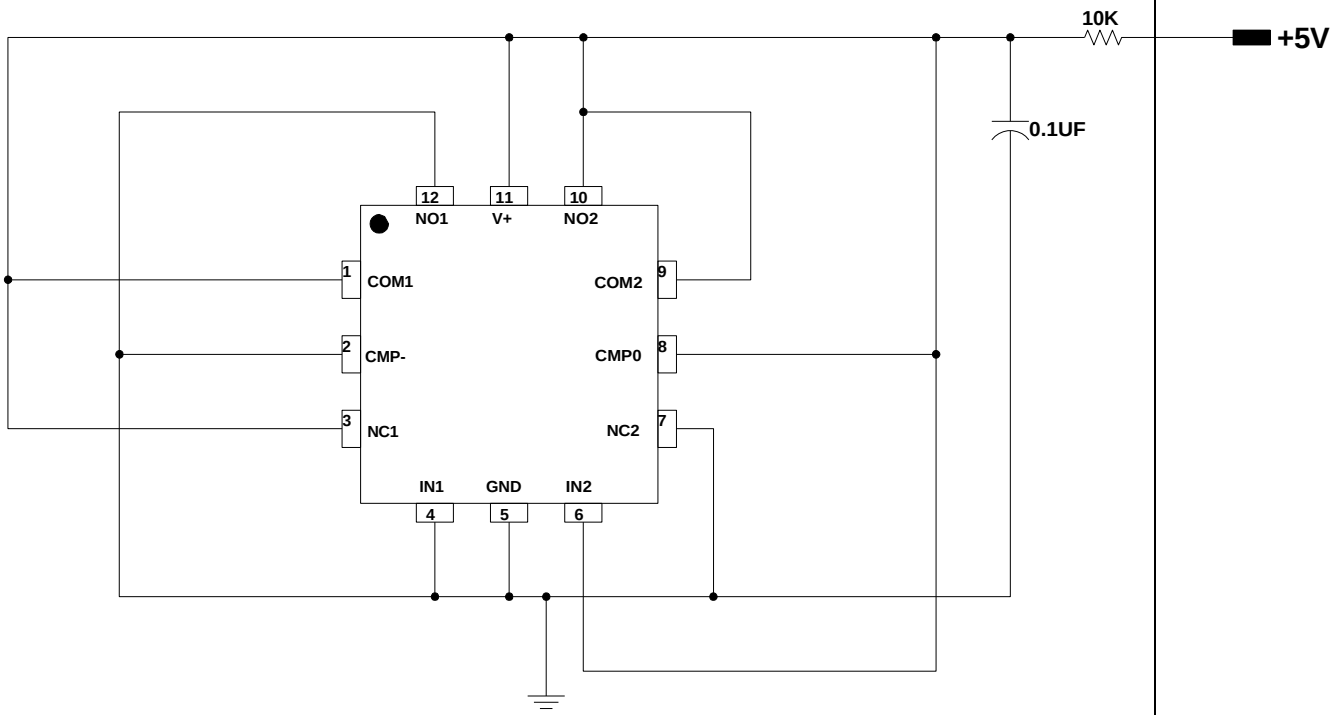


PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B12-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.			BOND DIAGRAM #: 05-9000-0965	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4765 (AS37Z)
PACKAGE: 12-QFN (4x4) THIN
MAX. EXPECTED CURRENT = 10uA

pedicord_j
2004-04-06 01:03:08

- DRAWN BY: TEK TAN
NOTES:

DRAWN BY: TEK TAN
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