RELIABILITY REPORT

FOR

MAX4758EBX+T

CHIP SCALE PACKAGE

January 18, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Don Lipps
Quality Assurance
Manager, Reliability Engineering

Conclusion

The MAX4758EBX+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4758/MAX4759 quad double-pole/double-throw (DPDT) analog switches operate from a single +1.8V to +5.5V supply. These switches feature low 0.5 on-resistance for audio switching and a low 25pF capacitance for data switching. The MAX4758 has eight 0.5 on-resistance switches to switch audio signals. The MAX4759 has four 0.5 on-resistance switches to route audio signals and four 25pF capacitance switches to route data signals. The MAX4758/MAX4759 have four logic inputs to control the switches in pairs. The MAX4758/MAX4759 are available in a small 36-pin (6mm x 6mm) thin QFN and 36-bump (3mm x 3mm) chip-scale package (UCSP(tm)).

II. Manufacturing Information

A. Description/Function:	Quad DPDT Audio/Data Switches in UCSP/QFN
B. Process:	E35
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	Dallas
F. Date of Initial Production:	July 14, 2004

III. Packaging Information

A. Package Type:	36-pin UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-0679
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	N/A
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	122 X 122 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm F.
Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the E35 Process results in a FIT Rate of 0.68 @ 25C and 11.68 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot CIB0AU001B, D/C 0331)

The AS27 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4758EBX+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	CIB0AU001B, DC 0331

Note 1: Life Test Data may represent plastic DIP qualification lots.