MAX4754ExE
Rev. A

RELIABILITY REPORT

FOR

MAX4754ExE

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

October 18, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Conclusion

The MAX4754 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4754 low on-resistance, analog switches operates from a single +1.8V to +5.5V supply. The MAX4754 is a dual, doublepole, double-throw (DPDT) switches.

The MAX4754 has four 0.5 ohm SPDT switches for audiosignal routing and two logic control inputs.

The MAX4754 is available in a space-saving 16-pin thin QFN and a tiny 16-bump 2mmx 2mm chip-scale package (UCSP™).

B. Absolute Maximum Ratings

Item	Rating
(All Voltages Referenced to GND)	
V+, IN_, EN	-0.3V to +6V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current	
NC1, NC2, COM1	±100mA
NO_, NC_, COM_ (remaining terminal connections)	±300mA
Peak Current NC1, NC2, COM1	
(Pulsed at 1ms, 10% duty cycle)	±200mA
(Pulsed at 1ms, 50% duty cycle)	±150mA
Peak Current NO_, NC_, COM__ (remaining terminal connections)	
(Pulsed at 1ms, 10% duty cycle)	±500mA
(Pulsed at 1ms, 50% duty cycle)	±400mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Bump Temperature (soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation(TA = +70°C)	
16-Lead Thin QFN	1349mW
16-Bump UCSP	660mW
Derates above +70°C	
16-Lead Thin QFN	16.9mW/°C
16-Bump UCSP	8.2mW/°C

Note 1: Signals on NO_, NC_, COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function: 0.5 Ohm Quad SPDT Switches in UCSP/QFN

B. Process: D35

C. Number of Device Transistors: 496

D. Fabrication Location: Dallas, USA

E. Assembly Location: Philippines, Thailand or USA

F. Date of Initial Production: July, 2003

III. Packaging Information

A. Package Type:	**16-Lead Thin QFN**	**16-Bump UCSP**
B. Lead Frame:	Copper	N/A
C. Lead Finish:	Solder Plate	N/A
D. Die Attach:	Silver-Filled Epoxy	N/A
E. Bondwire:	Gold (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-9000-0631	# 05-9000-0632
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

IV. Die Information

A. Dimensions: 83 x 83 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si/Coppper

D. Backside Metallization: None

E. Minimum Metal Width: Metal 1 .5 microns (as drawn), Metal 2/3 .7 microns (as drawn)

F. Minimum Metal Spacing: Metal 1 .6 microns (as drawn), Metal 2/3 .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4389 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.40 \times 10^{-9}$

$\lambda = 4.40$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6173) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AS07 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4754ExE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN UCSP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	QFN UCSP	77 N/A	0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010 (Note 3)	DC Parameters	QFN UCSP	77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

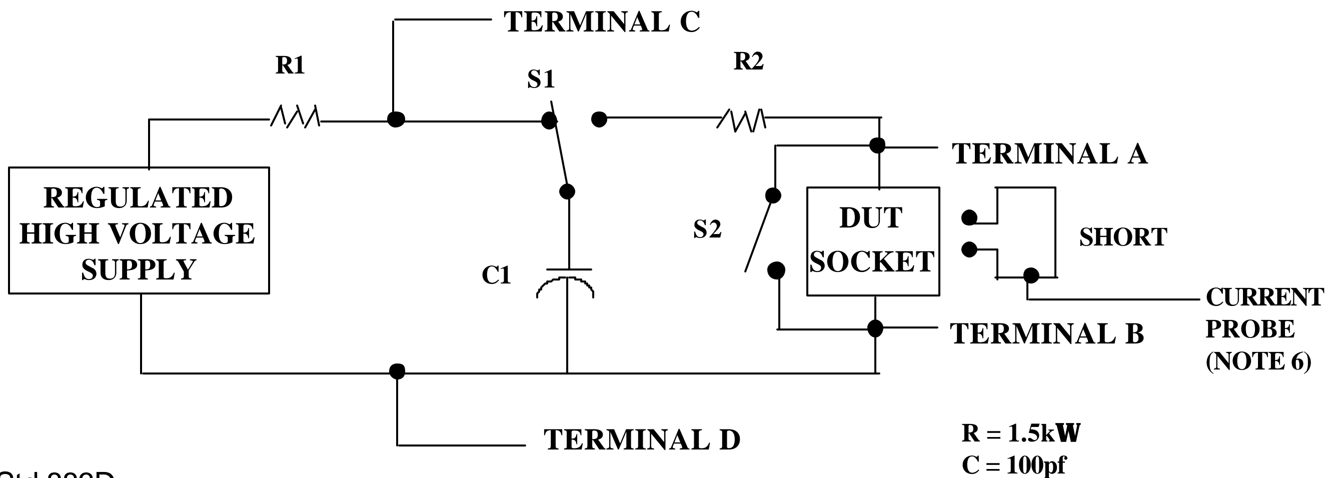
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

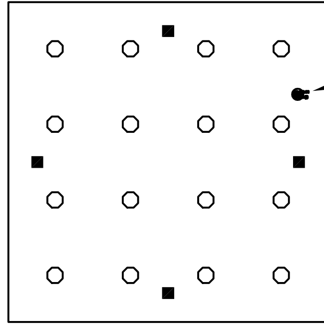
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



ORIGINAL CHIP

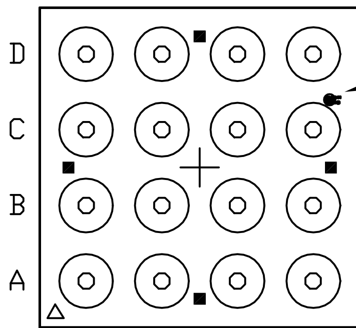


NORTH

WEST

EAST

AFTER BUMP

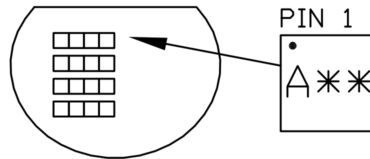


PIN 1

1 2 3 4

SOUTH

SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.

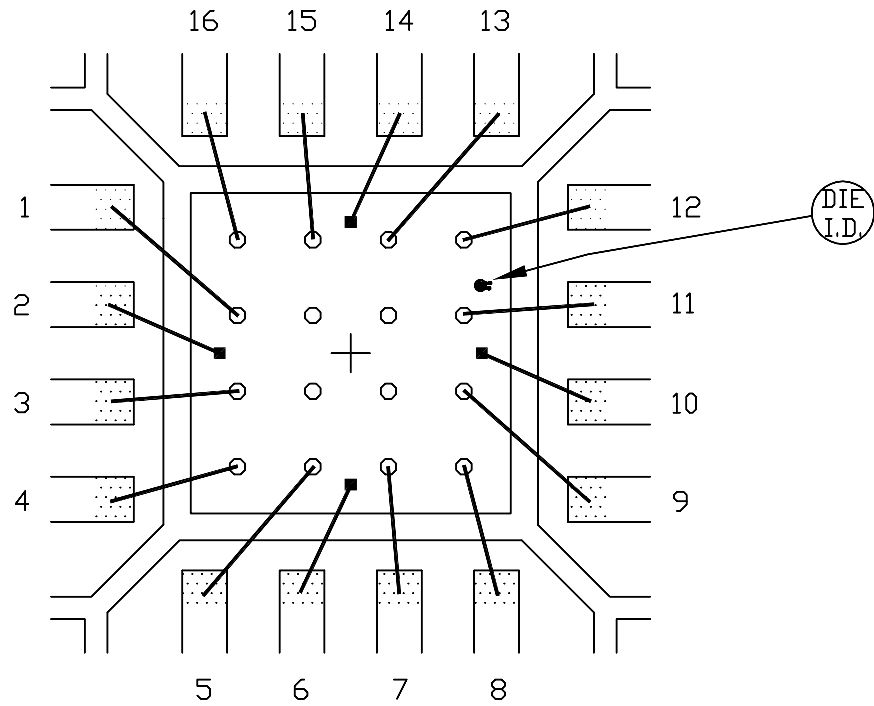


PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

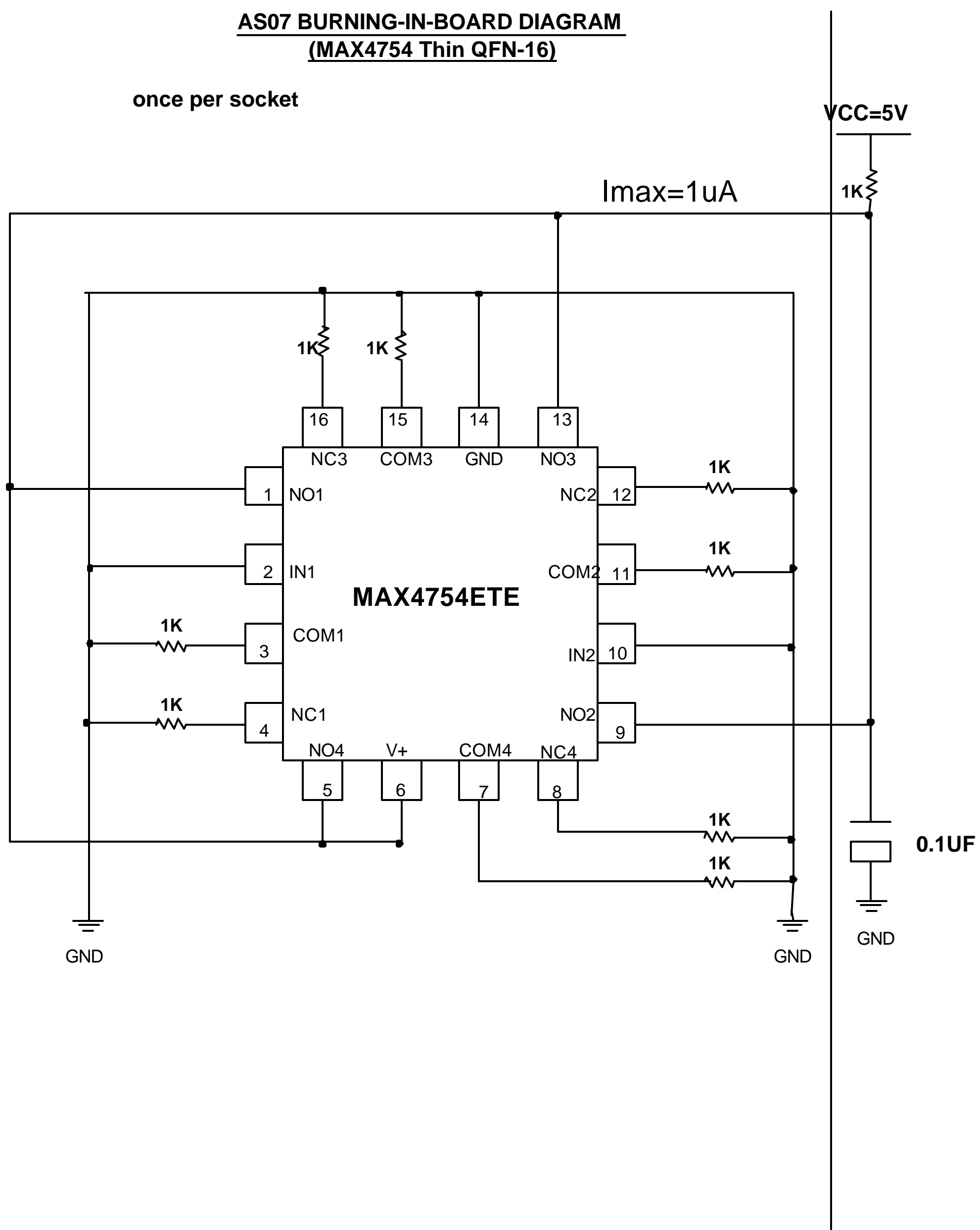
PKG. CODE: B16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.			BOND DIAGRAM #: 05-9000-0632	REV: A
	DESIGN				

4x4x0.8mm THIN QFN PKG.

EXPOSED PAD PKG.



PKG. CODE: T1644-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 98x98	PKG.			BOND DIAGRAM #: 05-9000-0631	REV: B
	DESIGN				



once per
board

DOCUMENT I.D. 06-6173	**REVISION** A	***MAXIM*** **TITLE: BI Circuit (MAX4754) AS07**	**PAGE** 2