



RELIABILITY REPORT  
FOR  
MAX4750EUD+  
PLASTIC ENCAPSULATED DEVICES

September 6, 2012

**MAXIM INTEGRATED PRODUCTS**

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<b>Approved by</b>
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## Conclusion

The MAX4750EUD+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX4747-MAX4750 low-voltage, quad single-pole single-throw (SPST)/dual single-pole/double-throw (SPDT) analog switches operate from a single +2V to +11V supply and handle rail-to-rail analog signals. These switches exhibit low leakage current (0.1nA) and consume less than 0.5nW (typ) of quiescent power, making them ideal for battery-powered applications. When powered from a +3V supply, these switches feature 50 (max) on-resistance ( $R_{ON}$ ), with 3.5 (max) matching between channels and 9 (max) flatness over the specified signal range. The MAX4747 has four normally open (NO) switches, the MAX4748 has four normally closed (NC) switches, and the MAX4749 has two N and two NC switches. The MAX4750 has two SPDT switches. These switches are available in 14-pin TSSOP, 16-pin TQFN (4mm x 4mm), and 16-bump WLP packages. This tiny chip-scale package occupies a 2mm x 2mm area and significantly reduces the required PC board area.

**II. Manufacturing Information**

A. Description/Function:	50 Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP
B. Process:	S3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	October 25, 2002

**III. Packaging Information**

A. Package Type:	14L TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0218 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	30°C/W
L. Multi Layer Theta Ja:	100.4°C/W
M. Multi Layer Theta Jc:	30°C/W

**IV. Die Information**

A. Dimensions:	80 X 80 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 43 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 25.5 \times 10^{-9}$$

$$\lambda = 25.5 \text{ F.I.T. (60\% confidence level @ } 25^{\circ}\text{C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S3 Process results in a FIT Rate of 0.04 @ 25C and 0.69 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot NBK3AQ001B D/C 0233)

The AS06-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX4750EUD+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	43	0	NBK0AQ001B, D/C 0233

Note 1: Life Test Data may represent plastic DIP qualification lots.