MAX4736Exx
Rev. A

# RELIABILITY REPORT

# FOR

# **MAX4736Exx**

# PLASTIC ENCAPSULATED DEVICES

October 23, 2008

# MAXIM INTEGRATED PRODUCTS

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## Conclusion

The MAX4736 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

## I. Device Description

### A. General

The MAX4736 is a low on-resistance, low-voltage, dual single-pole/double throw (SPDT) analog switch that operates from a single 1.6V to 4.2V supply. This device has fast switching speeds (tON = 25ns, tOFF = 20ns max), handles Rail-to-Rail® analog signals, and consumes less than 4µW of quiescent power. The MAX4736 has break-before-make switching.

When powered from a 3V supply, the MAX4736 features low 0.6∧ on-resistance (RON), with 0.1∧ RON matching and 0.05∧ RON flatness. The digital logic input is 1.8V CMOS compatible when using a single 3Vsupply.

The MAX4736 has one normally open (NO) switch and one normally closed (NC) switch, and is available in 12-pin thin QFN, 10-pin µMAX and 10 pin µDFN packages.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| (Voltages Referenced to GND) | |
| V+, IN_ | -0.3V to +4.6V |
| COM_, NO_, NC_ (Note 1) | -0.3V to (V+ + 0.3V) |
| Continuous Current COM_, NO_, NC_ | ±300mA |
| Continuous Current (all other pins) | ±20mA |
| Peak Current COM_, NO_, NC_(pulsed at 1ms 10% duty cycle) | ±500mA |
| Continuous Power Dissipation (TA = +70°C) | |
| 10-Pin µDFN (derate 5.3mW/°C above +70°C) | 423.7mW |
| 10-Pin µMAX (derate 5.6mW/°C above +70°C) | 444mW |
| 12-Pin TQFN (derate 14.7mW/°C above +70°C) | 1176mW |
| Operating Temperature Range | -40°C to +85°C |
| Maximum Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

**Note 1:** Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward current to maximum current rating.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch |
| B. Process: | TC35 |
| C. Number of Device Transistors: | 379 |
| D. Fabrication Location: | Taiwan |
| E. Assembly Location: | Malaysia, Thailand or Philippines |
| F. Date of Initial Production: | April, 2002 |

## III. Packaging Information

| | | | |
|---|---|---|---|
| A. Package Type: | **10-Lead uDFN** | **10-Pin uMAX** | **12-TQFN** |
| B. Lead Frame: | Copper | Copper | Copper |
| C. Lead Finish: | Solder Plate or 100% Matte Tin (all packages) | | |
| D. Die Attach: | Silver-Filled Epoxy | Silver-Filled Epoxy | Silver-Filled Epoxy |
| E. Bondwire: | Gold (1.0 mil dia.) | Gold (1.0 mil dia.) | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-9000-1767 | # 05-1201-0294 | # 05-9000-1248 |
| H. Flammability Rating: | Class UL94-V0 | | |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: | Level 1 | Level 1 | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 41 x 41 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal 1 = 0.5 / Metal 2 = 0.6 / Metal 3 = 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal 1 = 0.45 / Metal 2 = 0.5 / Metal 3 = 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times \underbrace{4389}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}} \times 80 \times 2} \text{(Chi square value for MTTF upper limit)}$$

$\lambda = 13.74 \times 10^{-9}$

$\lambda$ = 13.74 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5551) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the TC35 Process results in a FIT Rate of 0.28 @ 25C and 4.76 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The AH85-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

## Table 1

Reliability Evaluation Test Results

**MAX4736Exx**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 80 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | uDFN<br>uMAX<br>TQFN | 77<br>77<br>77 | 0<br>0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

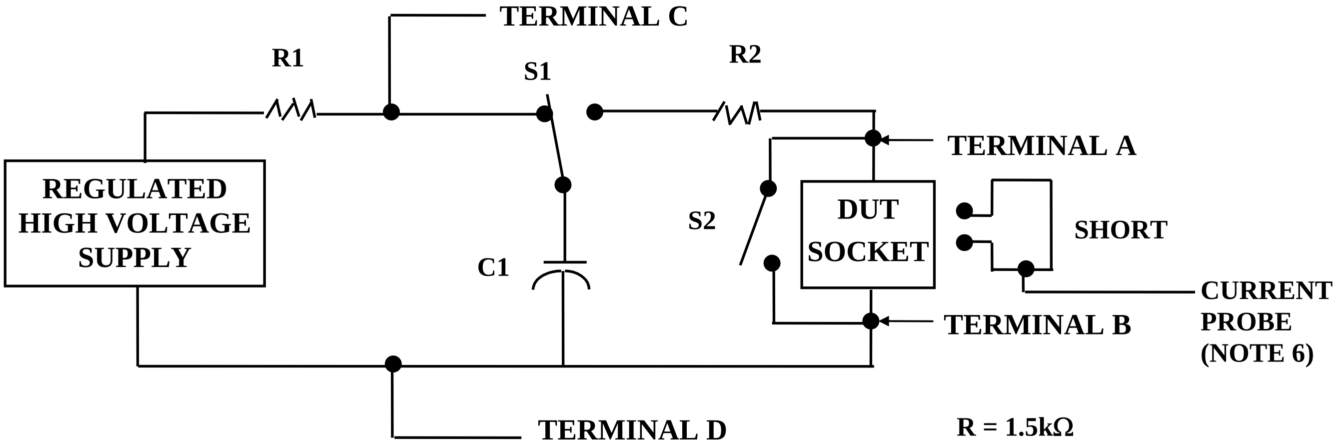
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



R = 1.5kΩ
C = 100pf