MAX4729ExT
Rev. A

RELIABILITY REPORT

FOR

MAX4729ExT

PLASTIC ENCAPSULATED DEVICES

May 25, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Conclusion

The MAX4729 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4729 single-pole/double-throw (SPDT) switches operate from a single supply ranging from +1.8V to +5.5V. These switches provide low 3.5Ω on-resistance (R_{ON}), as well as 0.45Ω R_{ON} flatness with a +2.7V supply. These devices typically consume only 1nA of supply current, making them ideal for use in lowpower, portable applications. The MAX4729 features low-leakage currents over the extended temperature range, TTL/CMOS-compatible digital logic, and excellent AC characteristics.

The MAX4729 is available in small 6-pin SC70 and 6-pin µDFN packages. The MAX4729 is offered in three pinout configurations to ease design. The MAX4729 is specified over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
(All voltages referenced to ground)	
V+, IN	-0.3V to +6V
COM, NO, NC (Note 1)	-0.3V to (V+ +0.3V)
Continuous Current (IN, V+, GND)	±30mA
Continuous Current (COM, NO, NC)	±80mA
Peak Current COM, NO, NC	
(Pulsed at 1ms, 10% Duty Cycle)	±150mA
Continuous Power Dissipation (TA = +70°C)	
6-Pin µDFN (derate 2.1mW/°C above +70°C)	168mW
6-Pin SC70 (derate 3.1mW/°C above +70°C)	245mW
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on NO, NC, or COM exceeding V+ or GND are clamped by internal diodes. Signals on IN exceeding GND are clamped by an internal diode. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	Low-Voltage 3.5Ω, SPDT,CMOS Analog Switches
B. Process:	D35/E35
C. Number of Device Transistors:	190
D. Fabrication Location:	Texas, USA
E. Assembly Location:	Thailand or Mayalsia
F. Date of Initial Production:	April, 2004

III. Packaging Information

	6-Pin uDFN (1.5x1)	**6-Pin SOT23**
A. Package Type:	**6-Pin uDFN (1.5x1)**	**6-Pin SOT23**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Non-Conductive Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1636	# 05-9000-0835
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	28 x 431 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.45 microns, Metal2 = 0.5 microns, Metal3 = 0.6 (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns, Metal2 = 0.5 microns, Metal3 = 0.6 (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 126 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 8.73 \times 10^{-9}$

λ = 8/73 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6251) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the D35/E35 Process results in a FIT Rate of 0.34 @ 25C and 5.69 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AS19-4 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

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Table 1
Reliability Evaluation Test Results

MAX4729Ext

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		126	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uDFN SOT	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

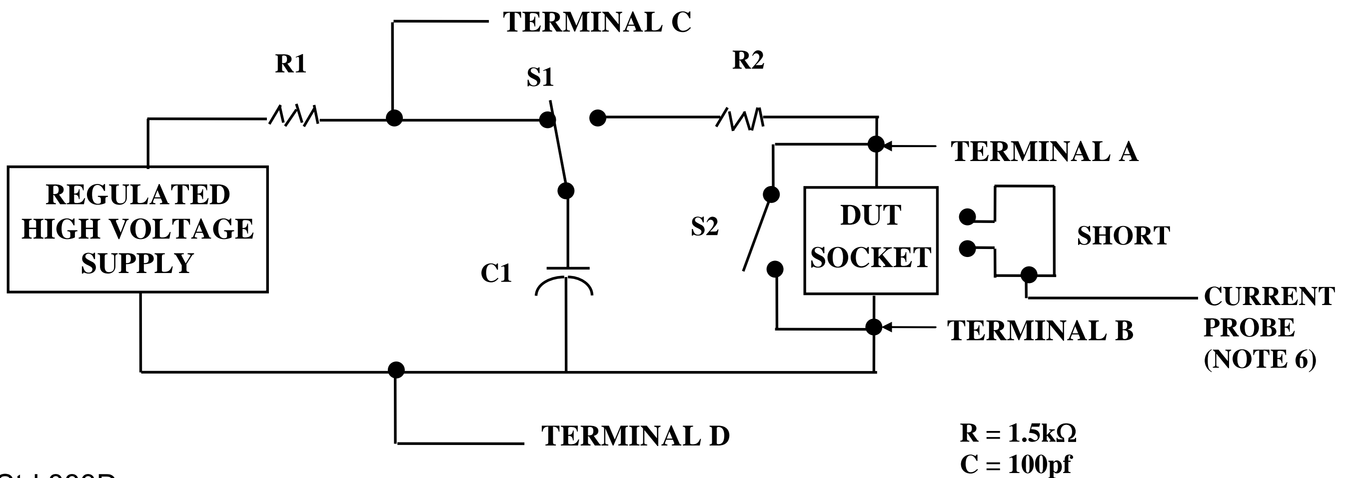
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S}$, $-V_{S}$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

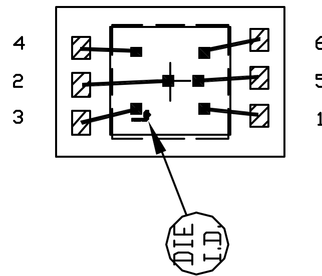
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

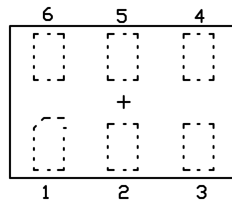


1.5x1.0x0.8mm uDFN

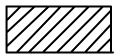
TOP VIEW

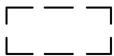


TOP VIEW OF BOTTOM LEADS

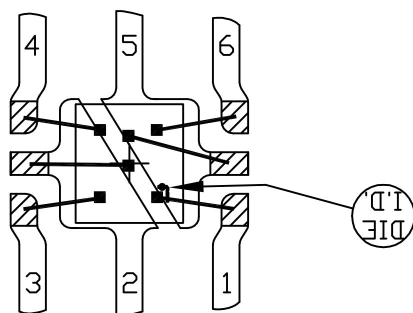


USE NON-CONDUCTIVE EPOXY

 BONDABLE AREA

 MAX. DIE PLACEMENT AREA

PKG. CODE: L611-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: - -	PKG.			BOND DIAGRAM #:	REV:
	DESIGN			05-9000-1636	B

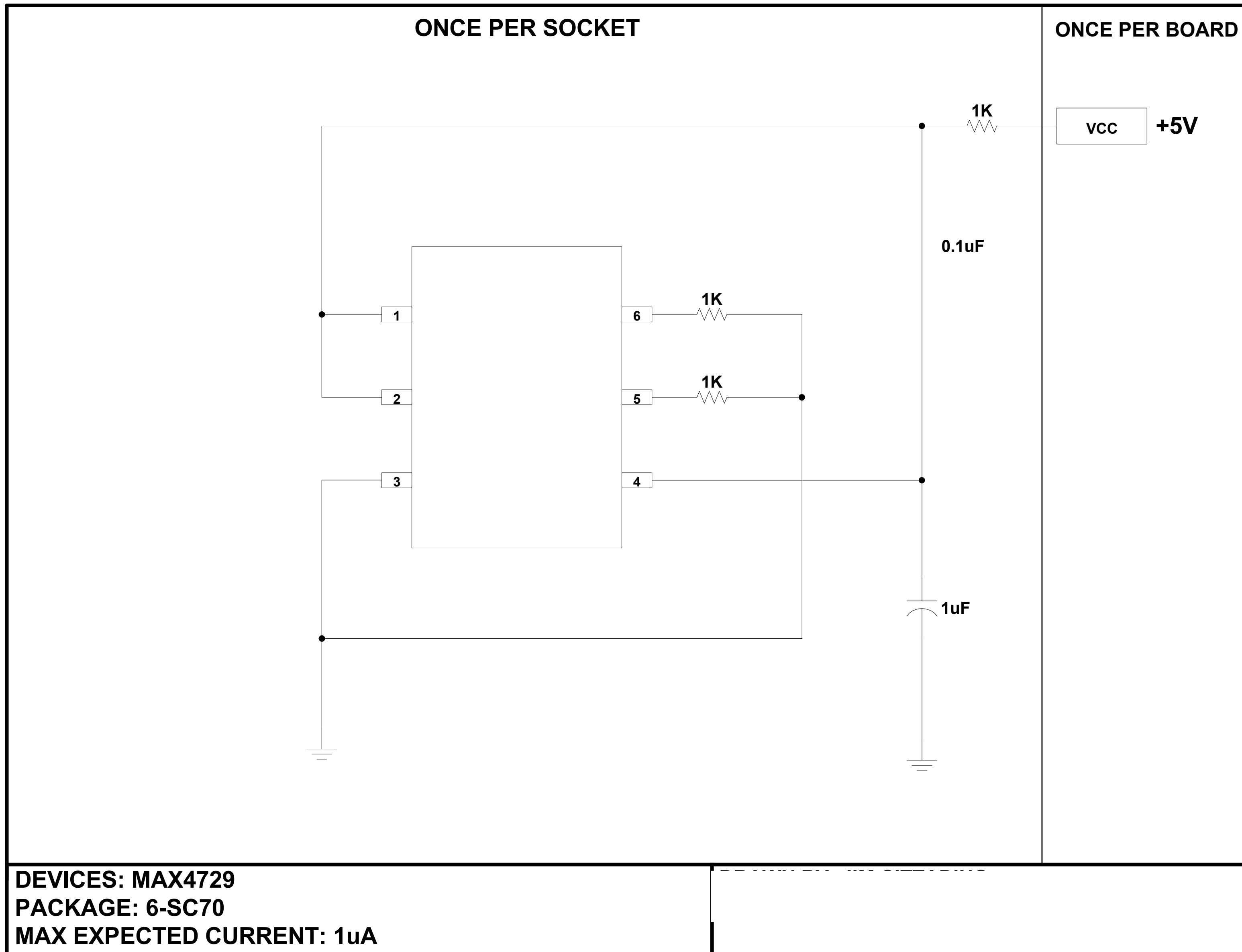


USE NON-CONDUCTIVE EPOXY ONLY

NOTE: CAVITY DOWN

BONDABLE AREA

PKG. CODE: X6S-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 36x34	PKG.			BOND DIAGRAM #: 05-9000-0835	REV: A
	DESIGN				



ONCE PER SOCKET
ONCE PER BOARD
1K
VCC
+5V
0.1uF
1K
1K
1
2
3
4
5
6
1uF
DEVICES: MAX4729
PACKAGE: 6-SC70
MAX EXPECTED CURRENT: 1uA