RELIABILITY REPORT

FOR

MAX4674ExE

PLASTIC ENCAPSULATED DEVICES

September 14, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4674 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4674 is a low-voltage CMOS analog switch containing four 2:1 multiplexers/demultiplexer. When powered from a single +5V supply, it features a low 4 ohm max on-resistance (RON), 0.4 ohm max RON matching between channels, and 0.8 ohm RON flatness over the entire signal range. Off-leakage current is only 0.5nA max at +25C.

The MAX4674 features fast turn-on (tON) and turn-off (tOFF) times of 18ns and 6ns, respectively, and is available in QSOP, TSSOP, and SO packages. This low-voltage multiplexer operates with a +1.8V to +5.5V single supply. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility with +5V operation.

B. Absolute Maximum Ratings

Item	Rating
V+, A0, EN	-0.3V to +6V
COM_, NO_, NC_ (Note1)	-0.3V to (V + 0.3V)
Continuous Current COM_, NO_, NC_	±100mA
Peak Current (COM_, NO_, NC_) (pulsed at 1ms, 10% duty cycle)	300mA
Continuous Power Dissipation	
16-Pin QSOP	667mW
16-Pin TSSOP	533mW
16-Pin Narrow SO	640mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C
16-Pin TSSOP	6.7mW/°C
16-Pin Narrow SO	8.0mW/°C
Die Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on NO_, NC_, and COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	3V/5V, 5Ω, Wideband Quad 2:1 Analog Multiplexer
B. Process:	TSMC05
C. Number of Device Transistors:	478
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines, Malaysia, Korea or Thailand
F. Date of Initial Production:	October, 2000

III. Packaging Information

A. Package Type:	**16-Lead QSOP**	**16-Lead TSSOP**	**16 Lead NSO**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0174	# 05-1201-0175	# 05-1201-0173
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	66 x 67 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	.5 micron as drawn
F. Minimum Metal Spacing:	.5 micron as drawn
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5573) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH43 die type has been found to have all pins able to withstand a transient pulse of ± 600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4674ExE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP TSSOP NSO	77 77 97	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

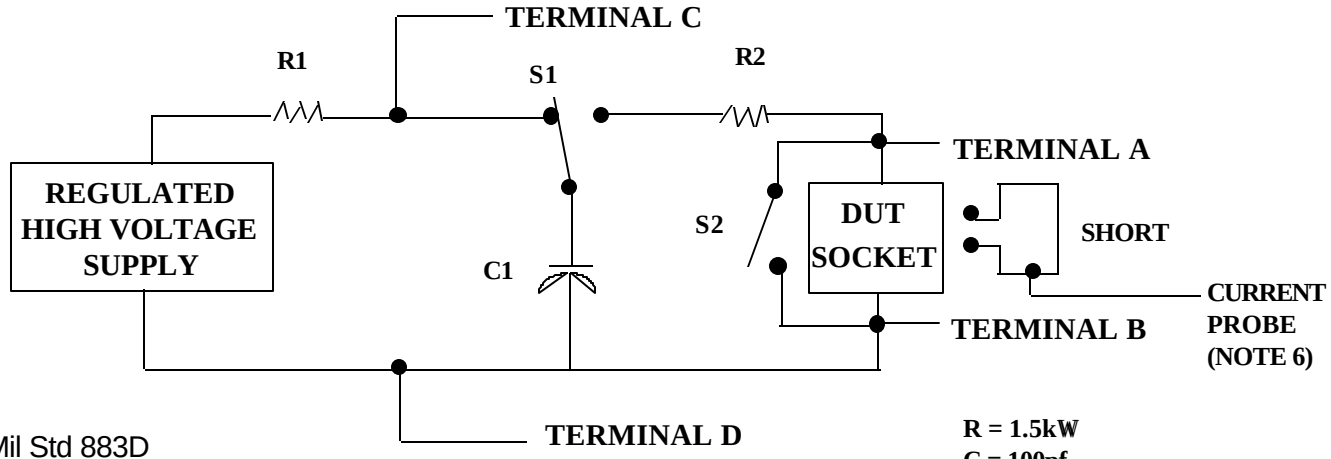
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

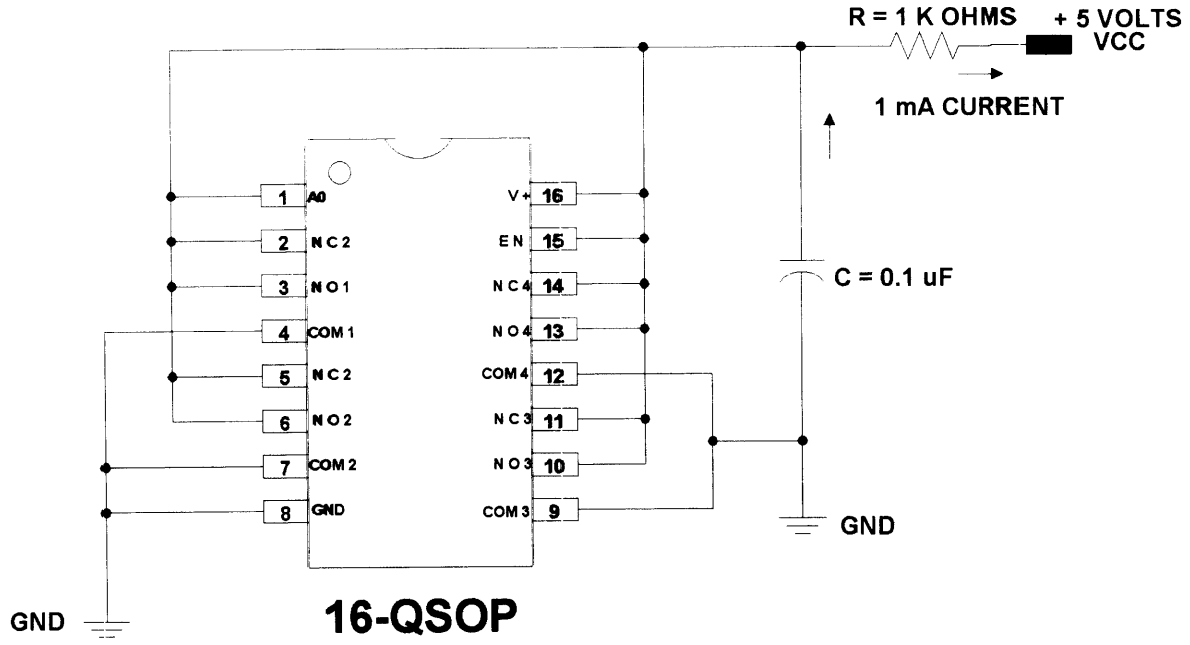
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

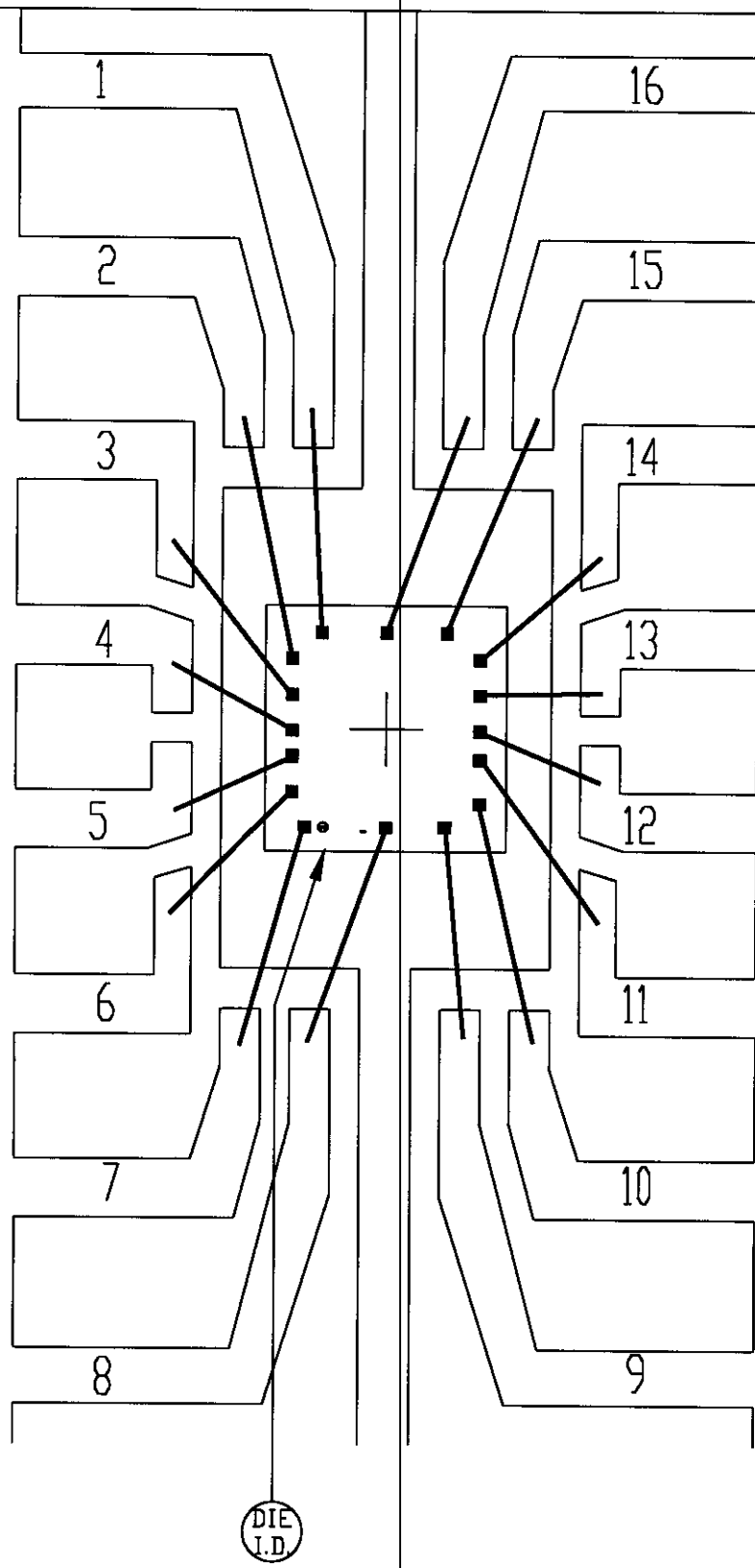
ONCE PER SOCKET

ONCE PER BOARD

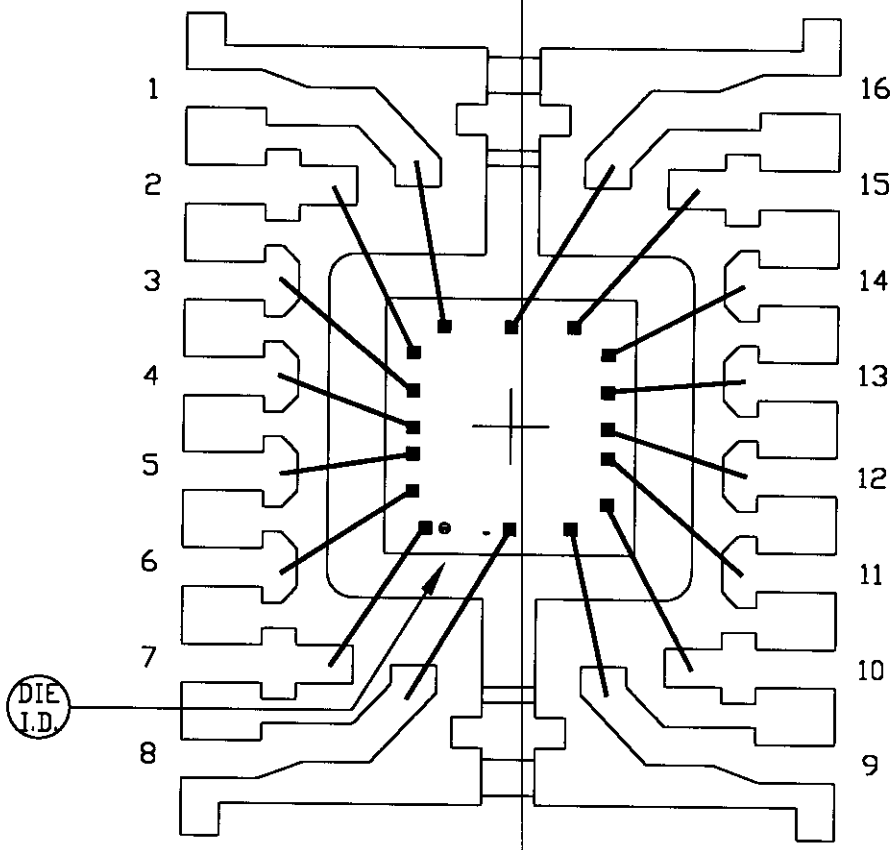


16-QSOP

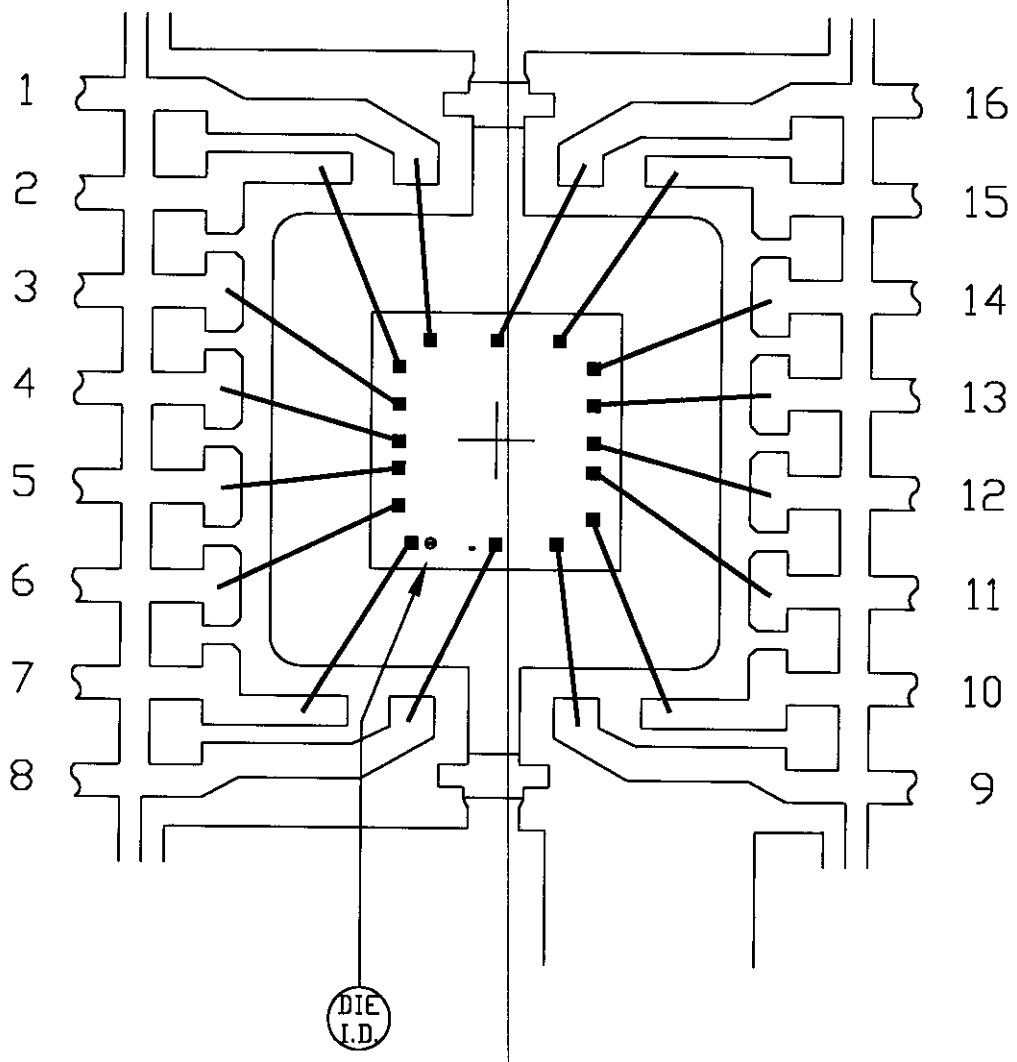
MAXIM BURN-IN SCHEMATIC SPEC 06-5573 REV. B DATE: 5/2 / 2000	DEVICES: MAX 4674 MAX. EXPECTED CURRENT = 100uA	NOTES:



PKG. CODE: S16-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 90 X 130	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0173 / REV: A



PKG. CODE: E16-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 96X90	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0174 / REV: A



PKG. CODE: U16-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 118X118	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0175 REV: A