RELIABILITY REPORT

FOR

MAX4624ExT

PLASTIC ENCAPSULATED DEVICES

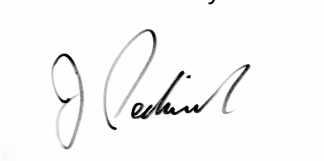
July 27, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

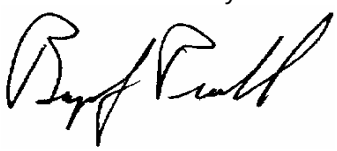
SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Managing Director

Conclusion

The MAX4624 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4264 is a low-on-resistance, low-voltage single-pole/double-throw (SPDT) analog switch that operates from a single +1.8V to +5.5V supply. The MAX4624 has break-before-make switching. This device also has fast switching speeds (t_{ON} = 50ns max, t_{OFF} = 50ns max).

When powered from a +5V supply, the MAX4624 offers 1Ω max on-resistance (R_{ON}), with 0.12Ω max R_{ON} matching and flatness. The digital logic input is TTL compatible when using a single +5V supply. This switch also features overcurrent protection to prevent damage from short circuits and excessive loads.

B. Absolute Maximum Ratings

Item	Rating
Voltages Referenced to GND	
V+, IN	-0.3V to +6V
COM, NC, NO (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current NO, NC to COM	±200mA
Peak Current NO, NC to COM (pulsed at 1ms, 10% duty cycle max)	±400mA
Junction Temperature	+150°C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23	571mW
6-Pin Thin SOT23	500mW
Derates above +70°C	
6-Pin SOT23	7.1mW/°C
6-Pin Thin SOT23	6.25mW/°C

II. Manufacturing Information

A. Description/Function:	1Ω, Low-Voltage, Single-Supply SPDT Analog Switch
B. Process:	TC06 (0.6 micron CMOS)
C. Number of Device Transistors:	186
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	January, 2000

III. Packaging Information

	6 Lead SOT-23	**6 Lead Thin SOT-23**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Non-Conductive Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0130	# 05-1201-0241
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	57 x 35 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1: 0.9 microns; Metal 2: 0.9 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1: 0.8 microns; Metal 2: 0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 90 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 12.22 \times 10^{-9}$ λ=12.22 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-5509.) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH25 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4624ExT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		90	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT SOT-Thin	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

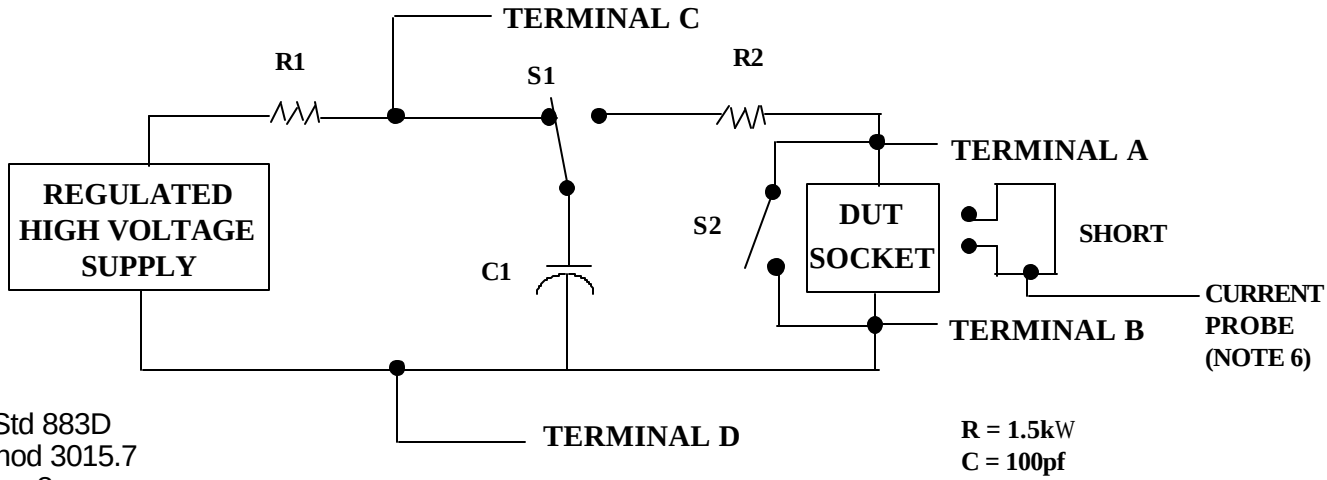
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

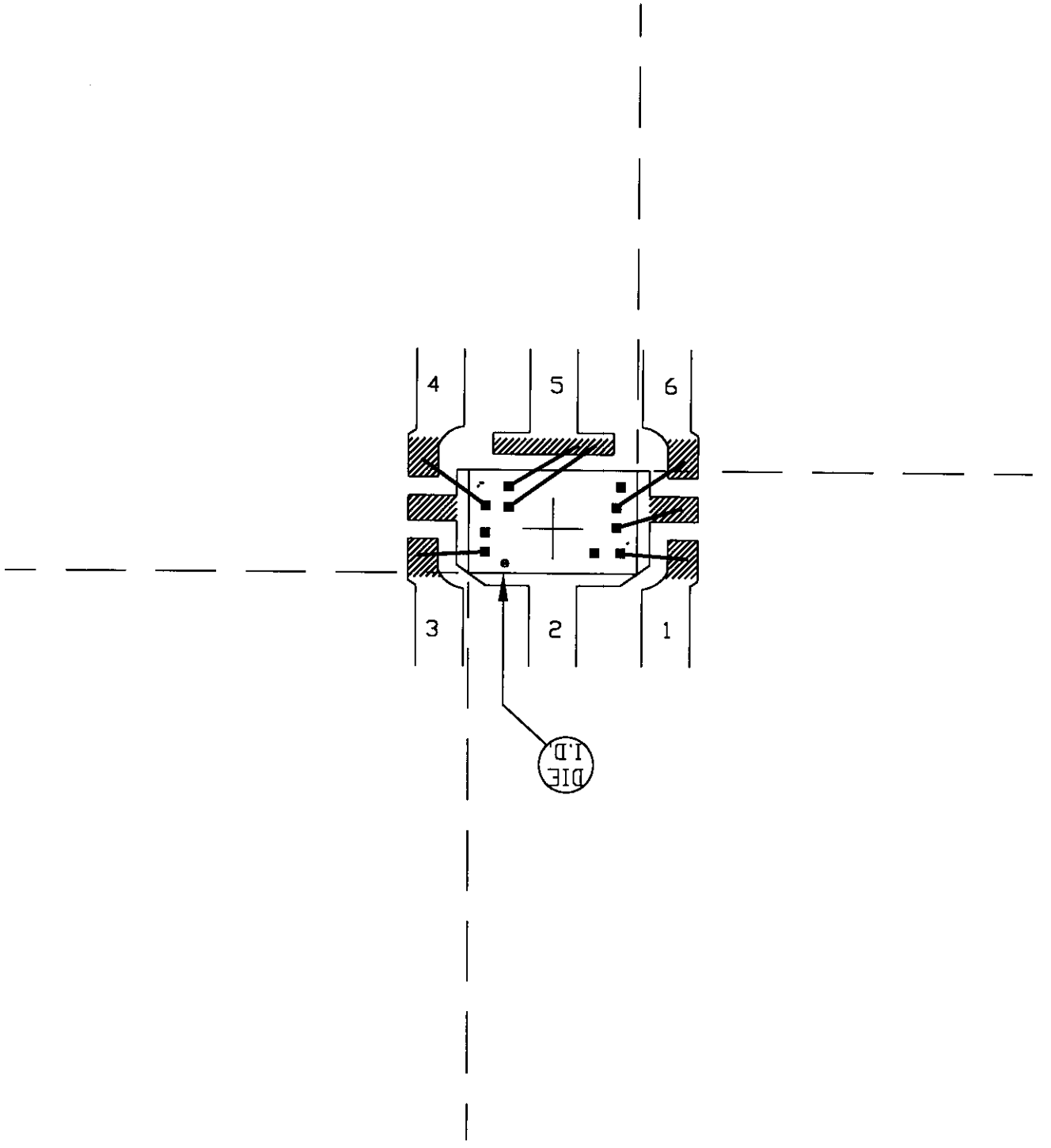
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



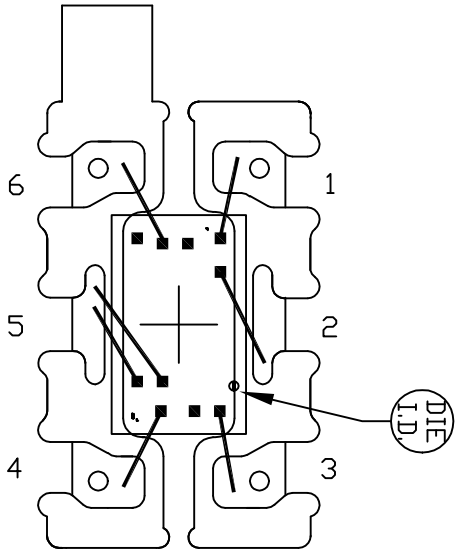
Mil Std 883D
Method 3015.7
Notice 8



NOTE: CAVITY DOWN

PKG.CODE: U6-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 64x38	PKG.		8/13/99	BUILDSHEET NUMBER: 05-1201-0130 REV.: A
	DESIGN		8/13/99	

THIN SOT PACKAGE

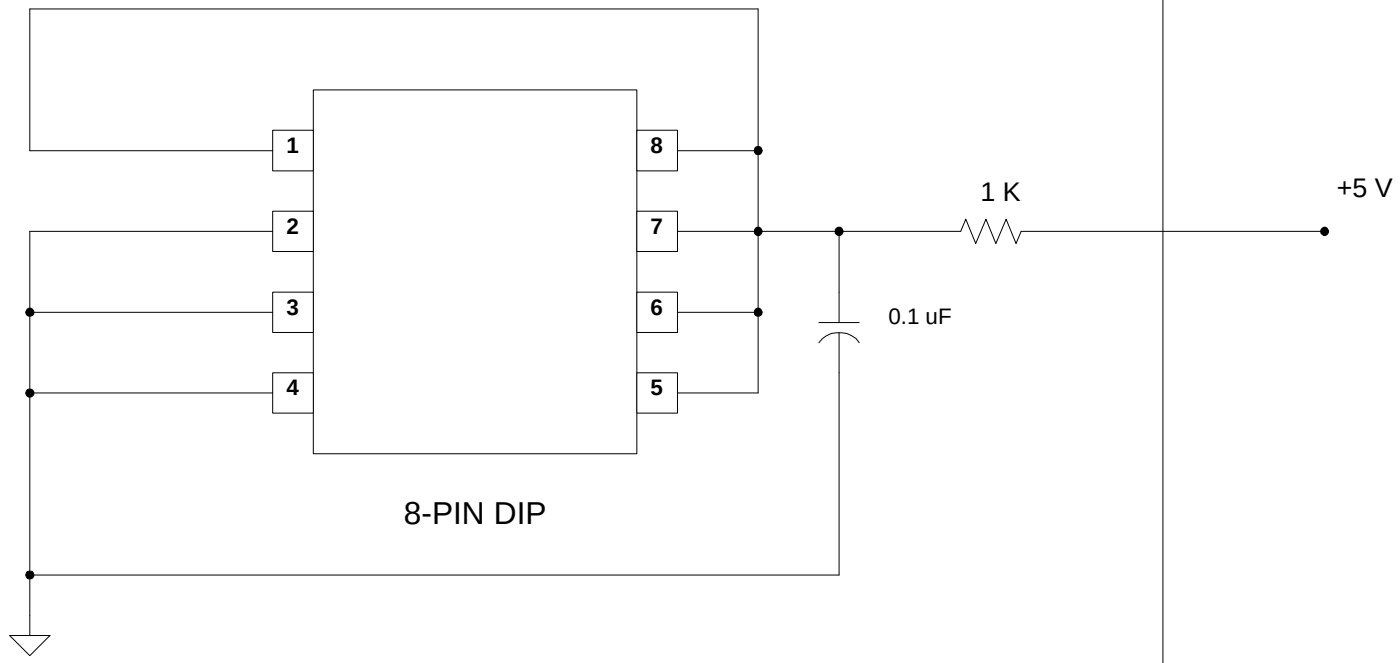


CAVITY DOWN

PKG. CODE: Z6-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 29x59	PKG.		3/2/01	BOND DIAGRAM #: 05-1201-0241 / REV: A
	DESIGN		3/5/01	

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX4624/4625/4641/4642/4643/4644/4724/4725
MAX. EXPECTED CURRENT = 100 uA

DRAWN BY: TODD BEJSOVEC
NOTES: