RELIABILITY REPORT

FOR

MAX4615xxD

PLASTIC ENCAPSULATED DEVICES

July 20, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4615 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation
IV. .....Die Information
.....Attachments

I. Device Description

A. General

The MAX4615 quad, low-voltage, high-speed, single-pole/single-throw (SPST) analog switch is pin compatible with the industry-standard 74HC4066/MAX4610 analog switch. On-resistance (10Ω max) is matched between switches to 1Ω max and is flat (1Ω max) over the specified signal range. The switch handles V+ to GND analog signal levels. Maximum off-leakage current is only 1nA at T_A = +25°C and 6nA at T_A = +85°C.

The MAX4615 has four normally closed (NC) switches. This CMOS switch operates from a single +2V to +5.5V supply. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

B. Absolute Maximum Ratings

Item	Rating
(Voltages referenced to GND)	
V+, IN_	-0.3V to +6V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.03V)
Continuous Current (any terminal)	±75mA
Peak Current (NO_, NC_, COM_)	
(pulsed at 1ms, 10% duty cycle)	±200mA
Operating Temperature Ranges	
MAX461_C_ _	0°C to +70°C
MAX461_E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
14-Pin TSSOP	500mW
14-Pin Narrow SO	640mW
14-Pin Plastic DIP	800mW
Derates above +70°C	
14-Pin TSSOP	6.3mW/°C
14-Pin Narrow SO	8.0mW/°C
14-Pin Plastic DIP	10.0mW/°C

Note 1: Signals on NO_, NC_, or COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches
B. Process:	TC06
C. Number of Device Transistors:	89
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand, Philippines or Malaysia
F. Date of Initial Production:	July, 1999

III. Packaging Information

A. Package Type:	**14-Pin TSSOP**	**14-Pin NSO**	**14-Pin PDIP**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0135	# 05-1201-0108	# 05-1201-0107
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	62 x 55 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1 - 0.9 microns / Metal 2 - 0.9 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1 - 0.9 microns / Metal 2 - 0.9 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 160 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 14.98 \times 10^{-9}$

$\lambda = 14.98$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5483) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AH23-1 die type has been found to have all pins able to withstand a transient pulse of ±200V Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4615xxD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP NSO TSSOP	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

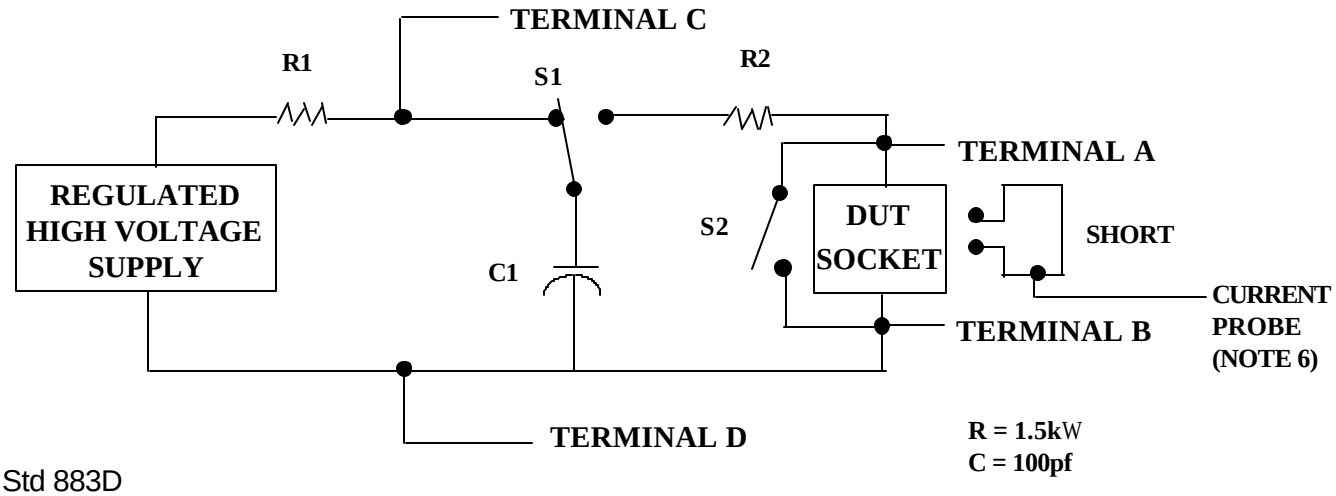
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

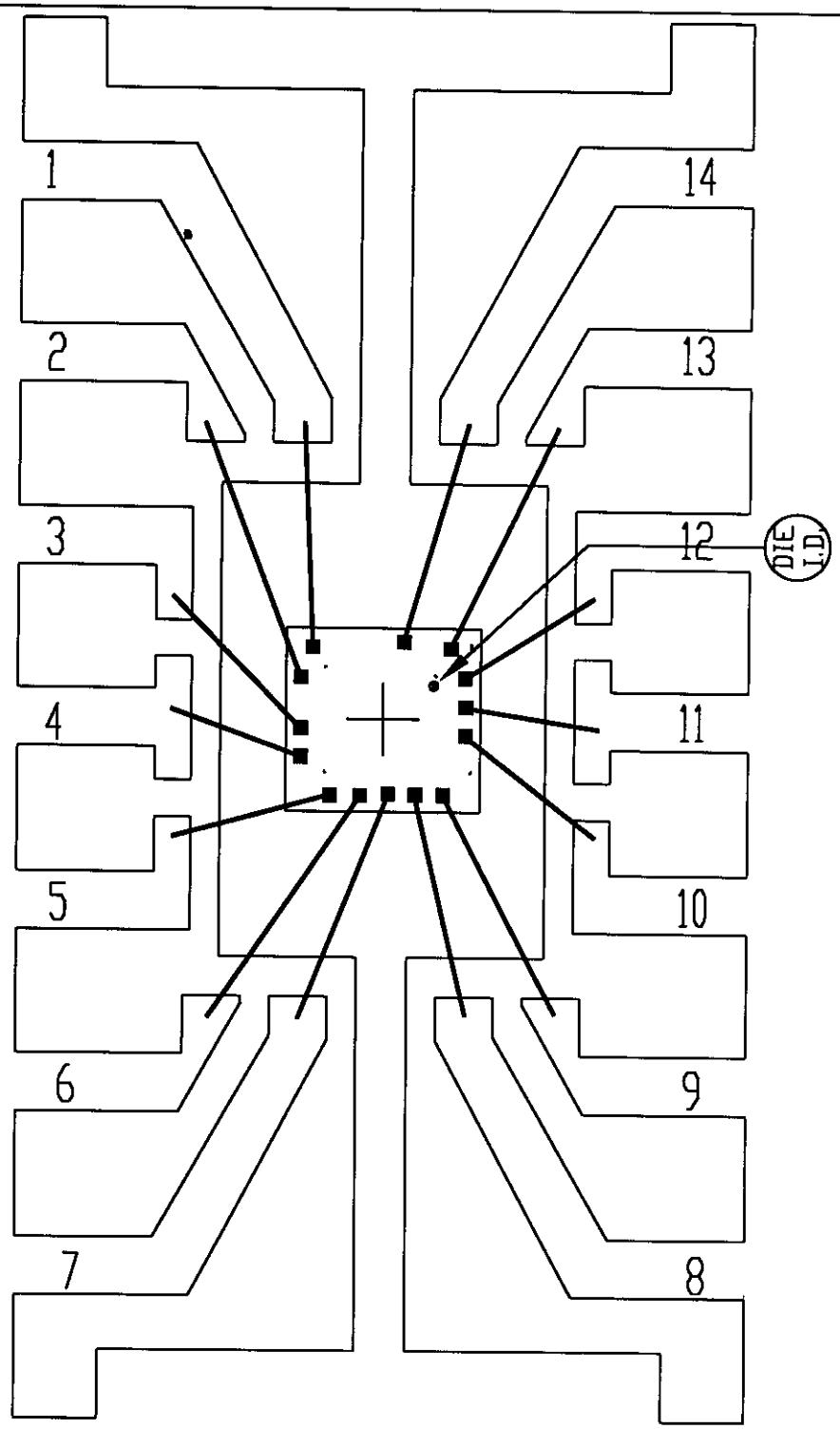
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

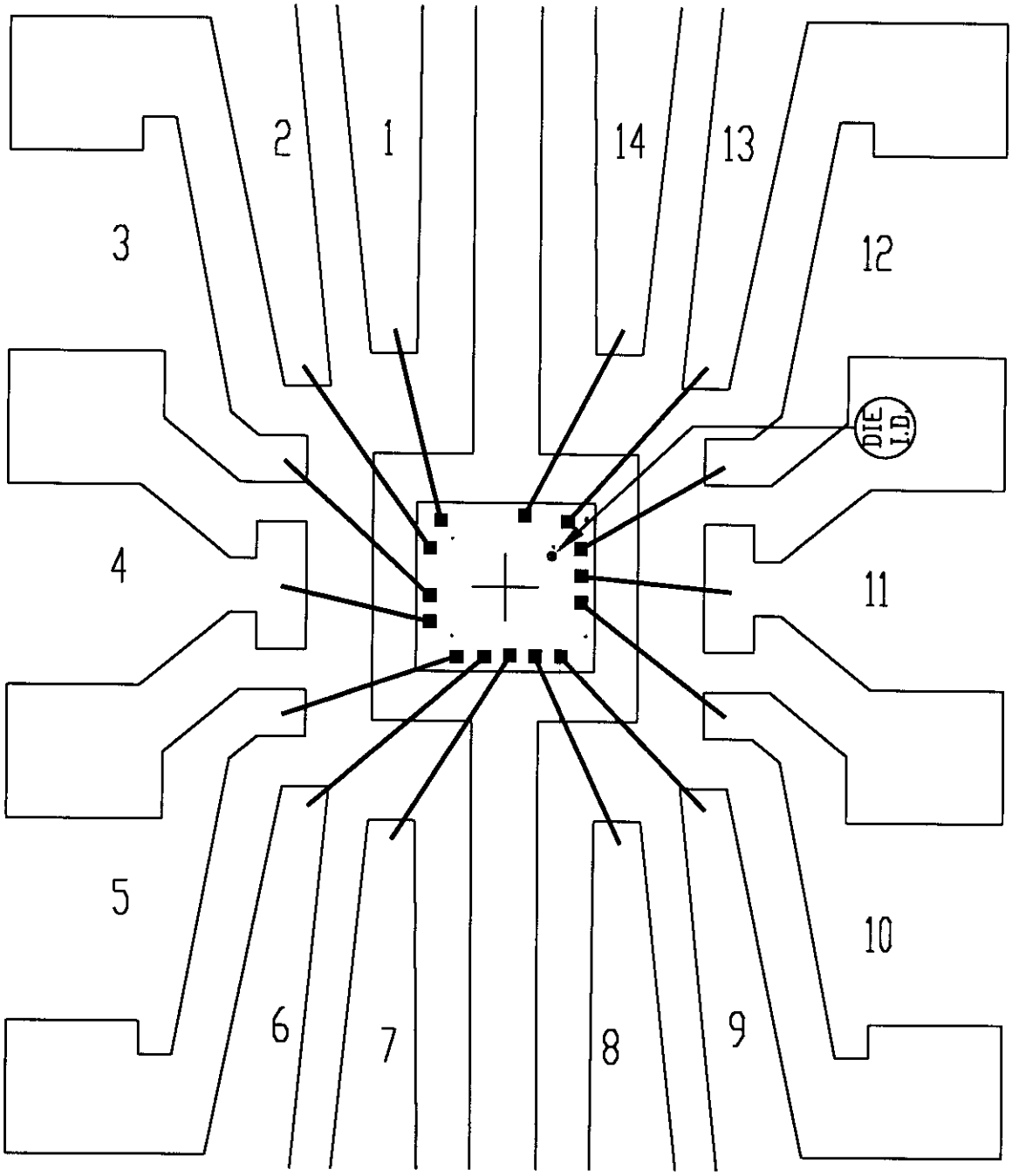
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: S14-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 90 X 130	PKG. DESIGN			BUILDSHEET NUMBER: 05-1201-0108 / REV.: A



PKG.CODE: P14-6		APPROVALS	DATE	MAXIM
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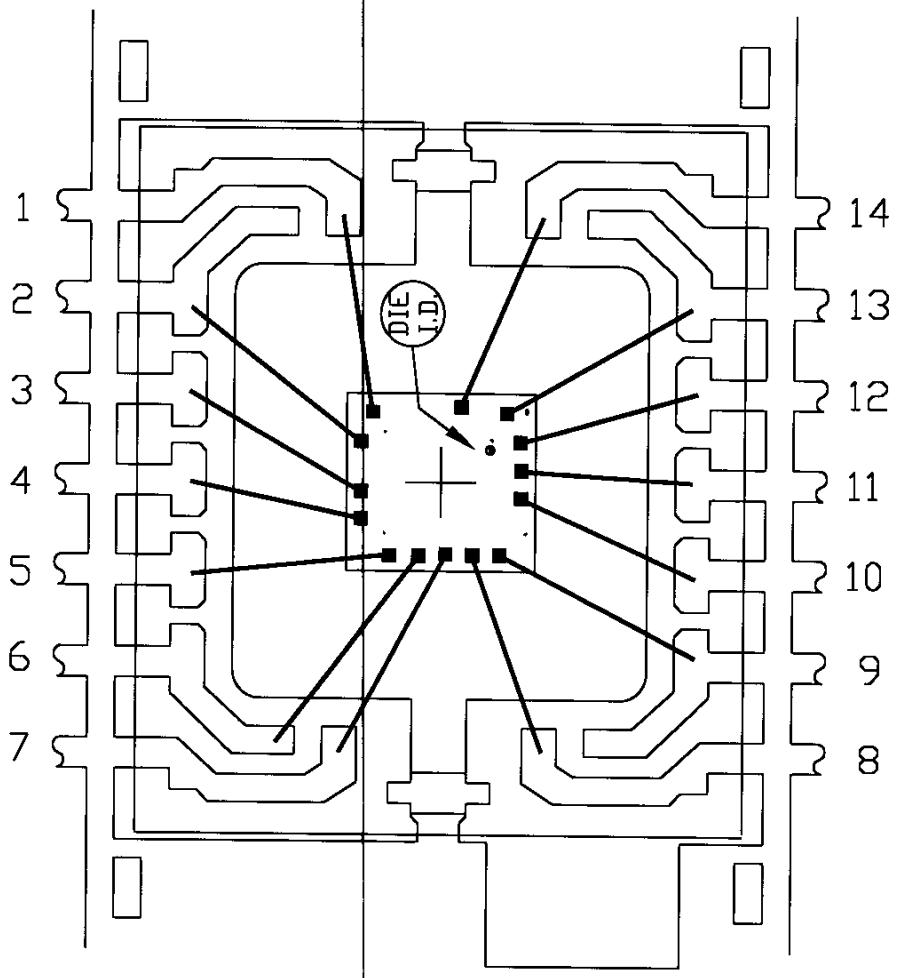

PKG.CODE: U14-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 118x122	PKG. DESIGN			BUILDSHEET NUMBER: 05-1201-0135 / REV.: A