

RELIABILITY REPORT FOR MAX4534EUD+ PLASTIC ENCAPSULATED DEVICES

January 4, 2011

# MAXIM INTEGRATED PRODUCTS

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SUNNYVALE, CA 94086

Approved by
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#### Conclusion

The MAX4534EUD+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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- I. Device Description
  - A. General

The MAX4534 (single 4-to-1) and MAX4535 (dual 2-to- 1) fault-protected multiplexers operate with ±4.5V to ±20V dual supplies or a +9V to +36V single supply. These multiplexers feature fault-protected inputs, rail-to-rail signal-handling capability, and overvoltage clamping at 150mV beyond the rails. Both parts feature ±40V overvoltage protection with supplies off and ±25V protection with supplies on. On-resistance is 400 max and is matched between channels to 10 max. All digital inputs have TTL logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +12V or dual ±15V supplies.



II. Manufacturing Information

Fault-Protected, High-Voltage, Single 4-to-1/Dual 2-to-1 Multiplexers

- A. Description/Function:
- B. Process:
- C. Number of Device Transistors:
- D. F abrication Location:
- E. Assembly Location:
- F. Date of Initial Production:

## III. Packaging Information

A. Package Type:	14-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1201-0142
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	30°C/W
L. Multi Layer Theta Ja:	100.4°C/W
M. Multi Layer Theta Jc:	30°C/W

S5

Oregon

January 22, 2000

Malaysia, Philippines, Thailand

#### IV. Die Information

Α.	Dimensions:	82 X 131 mils
В.	Passivation:	$Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)
C.	Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D.	Backside Metallization:	None
E.	Minimum Metal Width:	5.0 microns (as drawn)
F.	Minimum Metal Spacing:	5.0 microns (as drawn)
G.	Bondpad Dimensions:	5 mil. Sq.
Н.	Isolation Dielectric:	SiO <sub>2</sub>
Ι. Ι	Die Separation Method:	Wafer Saw



A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. S ampling Plan:	Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \times 4340 \times 80 \times 2}$  (Chi square value for MTTF upper limit)  $\lambda = 13.7 \times 10^{-9}$   $\lambda = 13.7 \text{ F.I.T.}$  (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.09 @ 25C and 1.55 @ 55C (0.8 eV, 60% UCL)

# B. E.S.D. and Latch-Up Testing (lot N3SAAQ001E D/C 9947)

The AH49 die type has been found to have all pins able to withstand a HBM transient pulse of +/-200V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.



# Table 1 Reliability Evaluation Test Results

# MAX4534EUD+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note	e 1) Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	N3SAAQ001E, D/C 9947

Note 1: Life Test Data may represent plastic DIP qualification lots.