



RELIABILITY REPORT  
FOR  
MAX4520EUA+  
PLASTIC ENCAPSULATED DEVICES

September 8, 2009

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

<b>Approved by</b>
Ken Wendel
Quality Assurance
Director, Reliability Engineering

## Conclusion

The MAX4520EUA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	IV. ....Die Information
.....Attachments	

## I. Device Description

### A. General

The MAX4510/MAX4520 single-pole/single-throw (SPST), fault-protected analog switches feature a fault-protected input and rail-to-rail signal-handling capability. The normally open (NO) and normally closed (NC) terminals are protected from overvoltage faults up to 36V during power-on and 44V with power off. During a fault condition, the switch input terminal (NO or NC) becomes an open circuit; only nanoamperes of leakage current flow from the fault source, and the switch output (COM) furnishes up to 13mA of the appropriate polarity supply voltage to the load. This ensures unambiguous rail-to-rail outputs when a fault begins and ends. On-resistance is 160  $\Omega$  max. The off-leakage current is only 0.5nA at +25°C and 10nA at +85°C. The MAX4510 is a normally closed switch, while the MAX4520 is a normally open switch. These CMOS switches operate with dual power supplies ranging from  $\pm 4.5V$  to  $\pm 20V$  or a single supply between +9V and +36V. The digital input has +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using  $\pm 15V$  or a single +12V supply. The MAX4510/MAX4520 are available in 6-pin SOT23 and 8-pin  $\mu$ MAX® packages.

## II. Manufacturing Information

A. Description/Function:	Rail-to-Rail, Fault-Protected, SPST Analog Switches
B. Process:	S5
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Thailand, Malaysia
F. Date of Initial Production:	October 19, 1999

## III. Packaging Information

A. Package Type:	8-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1201-0092
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	221°C/W
K. Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	206.3°C/W
M. Multi Layer Theta Jc:	41.9°C/W

## IV. Die Information

A. Dimensions:	57 X 38 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Ken Wendel (Director, Reliability Engineering)<br>Bryan Preeshl (Managing Director of QA)       |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 77 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 29.6 \times 10^{-9}$$

$$\lambda = 29.6 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.09 @ 25C and 1.55 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

### C. E.S.D. and Latch-Up Testing

The AH35-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-300V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX4520EUA+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	77	1
<b>Moisture Testing</b> (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data