RELIABILITY REPORT

FOR

MAX4511ESE+

PLASTIC ENCAPSULATED DEVICES

January 31, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Sokhom Chum
Quality Assurance
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Conclusion

The MAX4511ESE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4511/MAX4512/MAX4513 are quad, single-pole/single-throw (SPST), fault-protected analog switches. They are pin-compatible with the industry-standard nonprotected DG201/DG202/DG213. These new switches feature fault-protected inputs and rail-to-rail signal handling capability. The normally open (NO_) and normally closed (NC_) terminals are protected from overvoltage faults up to 36V during power-up or power-down. During a fault condition, the NO_ or NC_ terminal becomes an open circuit and only nanoamperes of leakage current flow from the source, but the switch output (COM_) furnishes up to 10mA of the appropriate polarity supply voltage to the load. This ensures unambiguous rail-to-rail outputs when a fault begins and ends. On-resistance is 175 max and is matched between switches to 10 max. The off-leakage current is only 0.5nA at +25°C and 10nA at +85°C. The MAX4511 has four normally closed switches. The MAX4512 has four normally open switches. The MAX4513 has two normally closed and two normally open switches. These CMOS switches can operate with dual power supplies ranging from ±4.5V to ±18V or a single supply between +9V and +36V. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±15V or a single +12V supply.

II. Manufacturing Information

A. Description/Function:	Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches
B. Process:	S5
C. Number of Device Transistors:	
D. F abrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	June 11, 1998

III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0301-0804
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	115°C/W
K. Single Layer Theta Jc:	32°C/W
L. Multi Layer Theta Ja:	N/A
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	86 X 138 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. B ackside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Is olation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. S ampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 100 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.0 \times 10^{-9}$

λ = 11.0 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.09 @ 25C and 1.55 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NQZAEN002A D/C 9904)

The AG76 die type has been found to have all pins able to withstand a HBM transient pulse of +/-400V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4511ESE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	100	0	NQZAEN002A, D/C 9904

Note 1: Life Test Data may represent plastic DIP qualification lots.