RELIABILITY REPORT

FOR

MAX4508xxE

PLASTIC ENCAPSULATED DEVICES

January 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4508 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4508 is a 8-to-1 fault-protected multiplexer that is pin compatible with the industry-standard DG508/ The MAX4508 operates with dual supplies of ±4.5V to ±20V or a single supply of +9V to +36V. This multiplexer features fault-protected inputs, Rail-to-Rail® signal handling capability, and overvoltage clamping at 150mV beyond the rails.

This parts offers ±40V overvoltage protection with supplies off and ±25V protection with supplies on. On-resistance is 400Ω max and is matched between channels to 15Ω max. All digital inputs have TTL logic thresholds, ensuring both TTL and CMOS logic compatibility when using a single +12V supply or dual ±15V supplies.

B. Absolute Maximum Ratings

Item	Rating
(Voltages Referenced to GND)	
V+	-0.3V to +44.0V
V-	-44.0V to +0.3V
V+ to V-	-0.3V to +44.0V
COM_, A_ (Note 1)	(V+ + 0.3V) to (V- - 0.3V)
NO	(V+ - 40V) to (V- + 40V)
NO_ to COM_	-36V to +36V
NO_ Overvoltage with Switch Power On	-30V to +30V
NO_ Overvoltage with Switch Power Off	-40V to +40V
Continuous Current into Any Terminal	±30mA
Peak Current, into Any Terminal	
(pulsed at 1ms, 10% duty cycle)	±100mA
Operating Temperature Ranges	
MAX4508C__	0°C to +70°C
MAX4508E__	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
1 6-Pin SO	471mW
1 6-Pin PDIP	842mW
Derates above +70°C	
16-Pin SO	8.70mW/°C
16-Pin PDIP	10.53mW/°C

Note 1: COM_, EN, and A_ pins are not fault protected. Signals on COM_, EN, or A_ exceeding V+ or V- are clamped by internaldiodes. Limit forward diode current to maximum current rating. (Voltages referenced to GND)

II. Manufacturing Information

A. Description/Function:	Fault-Protected, High-Voltage Single 8-to-1Multiplexers with Output Clamps
B. Process:	S5HV/MV2 – Medium Voltage 5 micron silicon gate CMOS
C. Number of Device Transistors:	543
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	January, 1999

III. Packaging Information

	16-Pin SO	**16-Pin PDIP**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-0301-0845	Buildsheet # 05-0301-0843
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	86 x 198 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contact: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 240 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.52 \times 10^{-9}$ $\lambda = 4.52$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0857) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AG85 die type has been found to have all pins able to withstand a transient pulse of 400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1

Reliability Evaluation Test Results

MAX4508xxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SO PDIP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

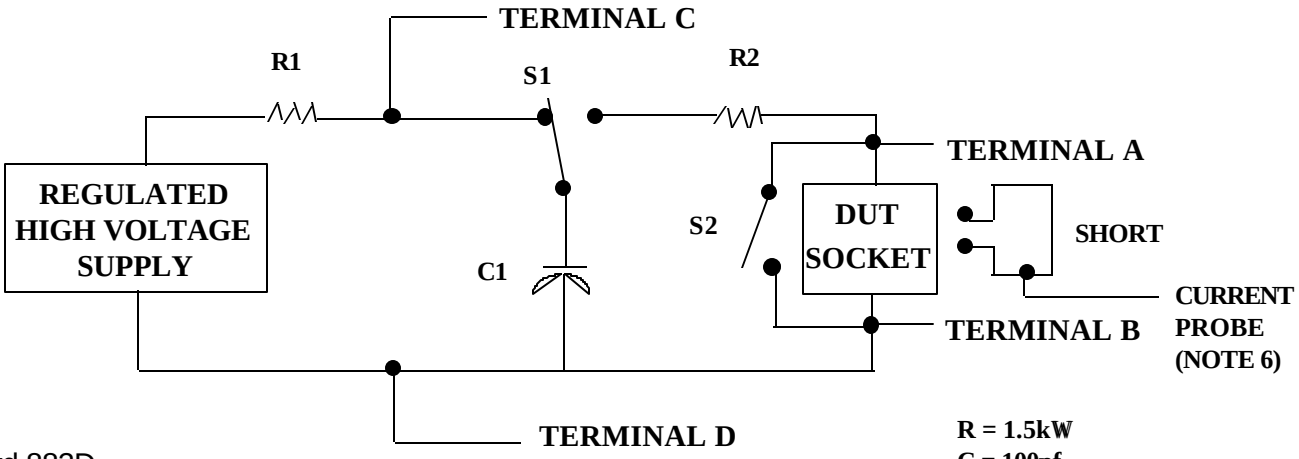
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

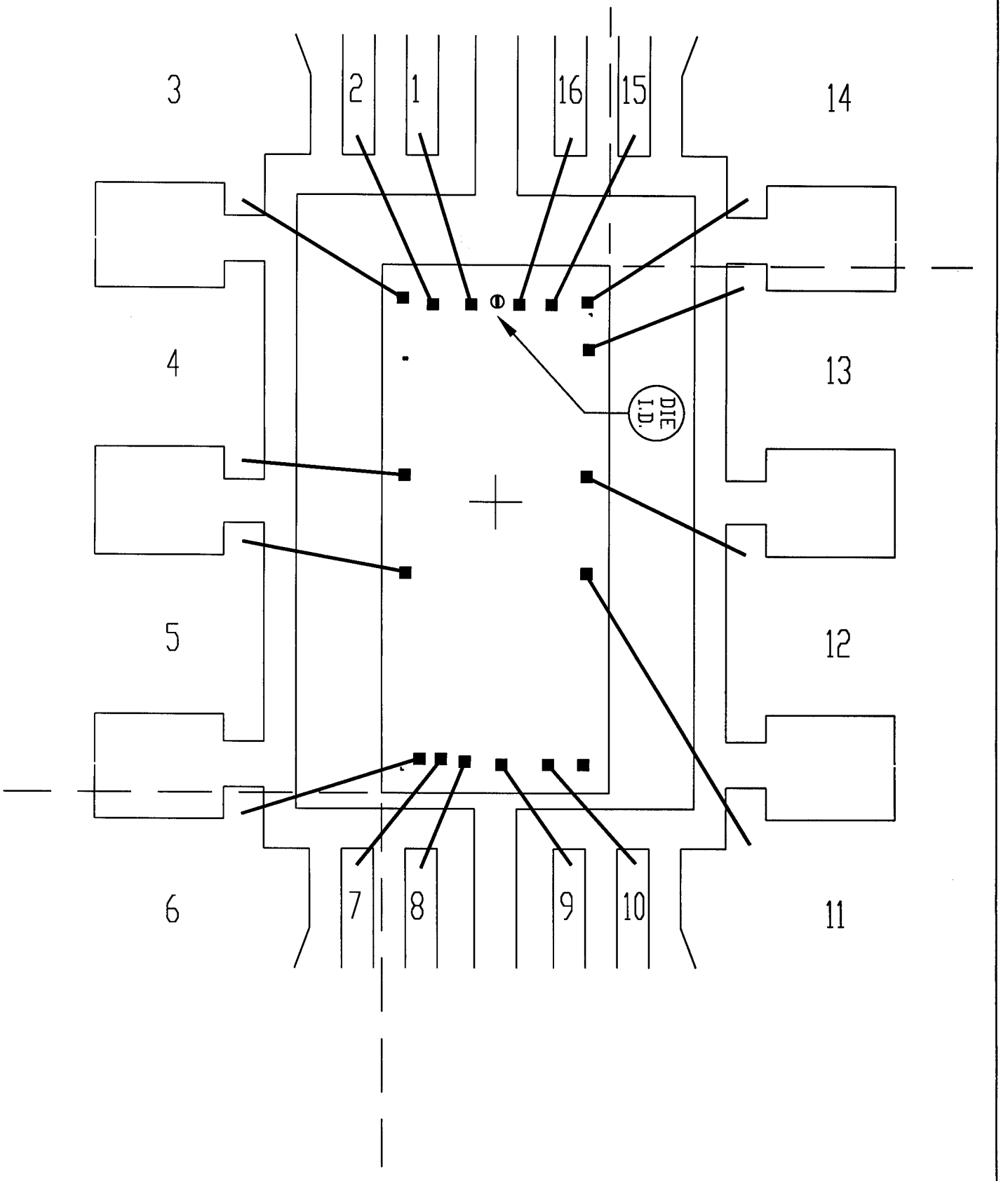
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

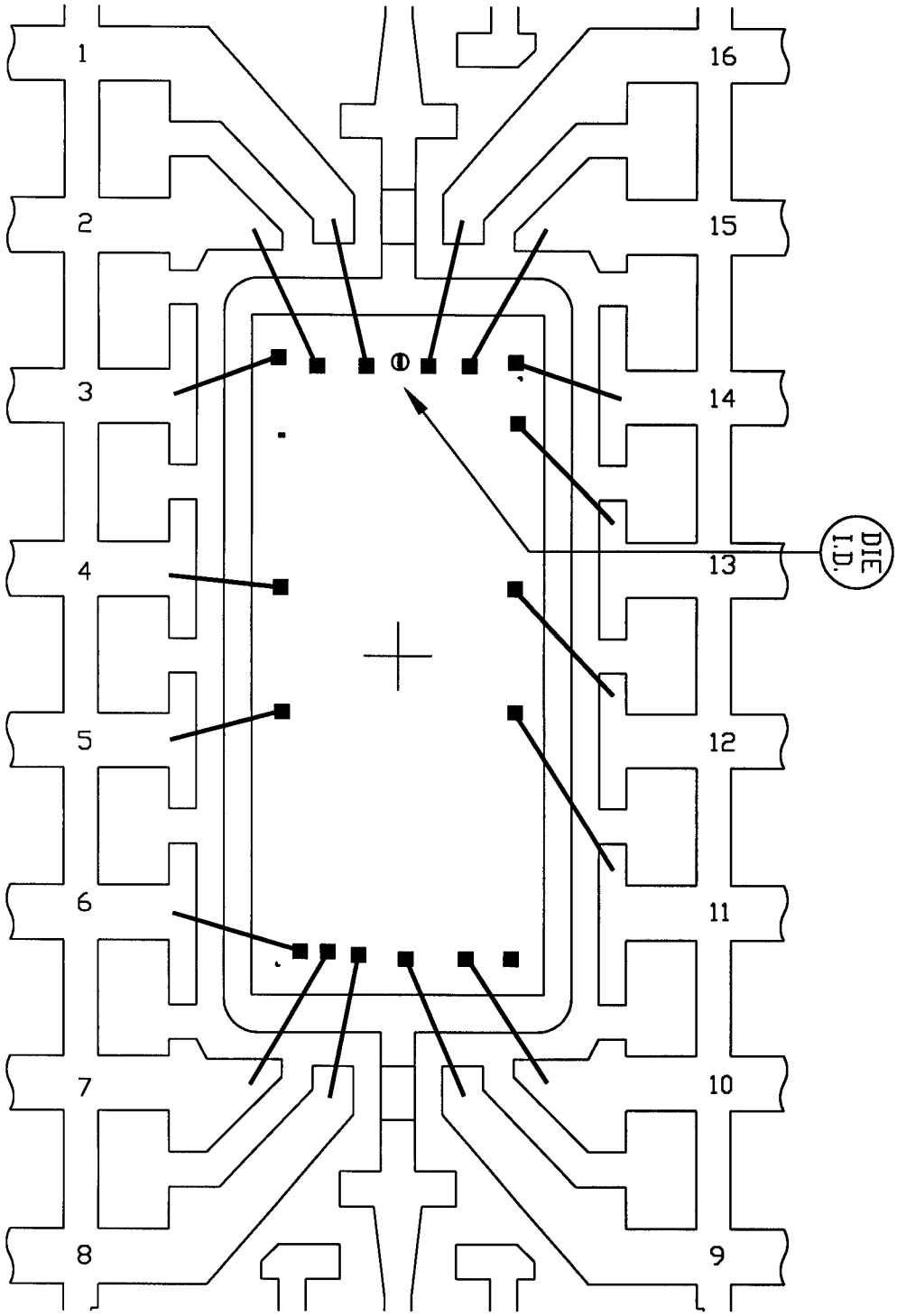
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



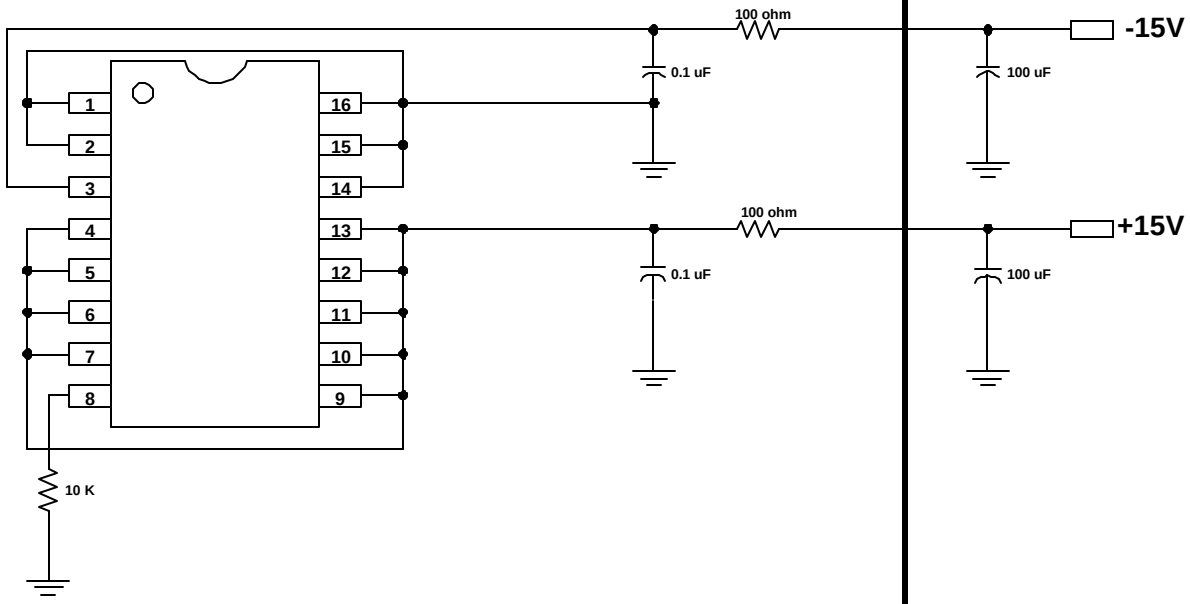
PKG.CODE: P16-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 150 X 230	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0843 / REV.: A



PKG.CODE: S16-8		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 102X220	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0845 / REV.: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 308/328/338/358/378/354/4708 DG 408/508 IH6108 MAX4508/HI1-0508A-2. PACKAGE: 16-DIP
Max current:(+/-15v) 50uA. For MAX4508/4708 Max current = 350uA.

DRAWN BY: HAK TAN

NOTES: