RELIABILITY REPORT

FOR

MAX4505EUK+T

PLASTIC ENCAPSULATED DEVICES

April 18, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineer

Conclusion

The MAX4505EUK+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4505 is a single signal-line protector featuring a fault-protected input and rail-to-rail signal handling capability. The input is protected from overvoltage faults up to ±36V with power on or ±40V with power off. During a fault condition, the input terminal becomes an open circuit and only nanoamperes of leakage current flow from the source, while the switch output (AOUT) furnishes typically 19mA from the appropriate polarity supply to the load. This ensures an unambiguous rail-to-rail output when a fault begins and ends. The MAX4505 protects both unipolar and bipolar analog signals using either unipolar (+9V to +36V) or bipolar (±8V to ±18V) power supplies. The device has no logic control inputs; the protector is always on when the supplies are on. On-resistance is 100 max, and on-leakage is less than 0.5nA at TA = +25°C. The MAX4505 is available in 5-pin SOT23 and 8-pin µMAX® packages.

II. Manufacturing Information

A. Description/Function:	Fault-Protected, High-Voltage, Signal Line Protector
B. Process:	S5
C. Number of Device Transistors:	56
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	July 24, 1999

III. Packaging Information

A. Package Type:	5-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1201-0127
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	324.3°C/W
K. Single Layer Theta Jc:	82°C/W
L. Multi Layer Theta Ja:	255.9°C/W
M. Multi Layer Theta Jc:	81°C/W

IV. Die Information

A. Dimensions:	38X56 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S5 Process results in a FIT Rate of 0.09 @ 25°C and 1.55 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AH34 die type has been found to have all pins able to withstand an HBM transient pulse of <400 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX4505EUK+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.