RELIABILITY REPORT

FOR

MAX4502xxx

PLASTIC ENCAPSULATED DEVICES

April 15, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4502 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4502 is a single-pole/single-throw (SPST), low-voltage, single-supply, CMOS analog switch. The MAX4502 is normally closed (NC).

This CMOS switch can operate continuously with a single supply between +2V and +12V. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1.0nA at +25°C or 10nA at +85°C.

The digital input has 0.8V and 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

B. Absolute Maximum Ratings

Item	Rating
(Voltages Referenced to GND)	
V+	-0.3V, +13V
Voltage into Any Terminal (Note 1)	-0.3V to (V+ +0.3V) or ±10mA (whichever occurs first)
Continuous Current into Any Terminal	±10mA
Peak Current, NO_ or COM_ (pulsed at 1ms, 10% duty cycle)	±20mA
ESD per Method 3015.7	>2000V
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation	
5-Lead SOT23	571mW
8-Lead SO	471mW
8-Lead PDIP	727mW
Derates above +70°C	
5-Lead SOT23	7.1mW/°C
8-Lead SO	5.88mW/°C
8-Lead PDIP	9.09mW/°C

Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	Low-Voltage, SPST, CMOS Analog Switch
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	17
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines or Thailand
F. Date of Initial Production:	April, 1996

III. Packaging Information

	5 Lead SOT-23	**8-Lead PDIP**	**8-Lead SO**
A. Package Type:			
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Non-Conductive Epoxy	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0301-0766	# 05-0301-0764	# 05-0301-0765
H. Flammability Rating:	Class UL94-V0		
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	31 x 29 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 237 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.58 \times 10^{-9}$

$\lambda = 4.58$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5174) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AG80-1 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX4502xxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		273	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP SO SOT23	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

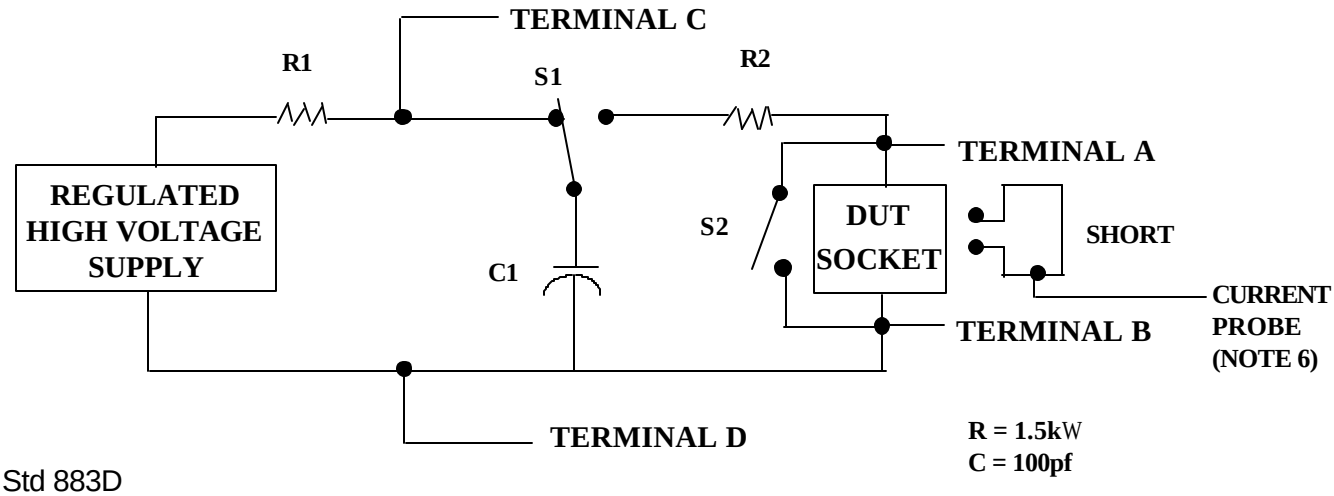
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

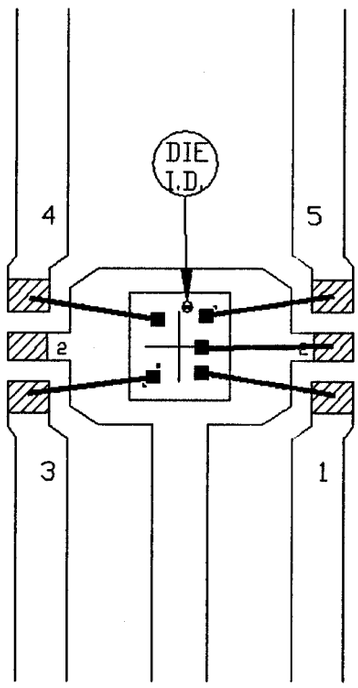
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

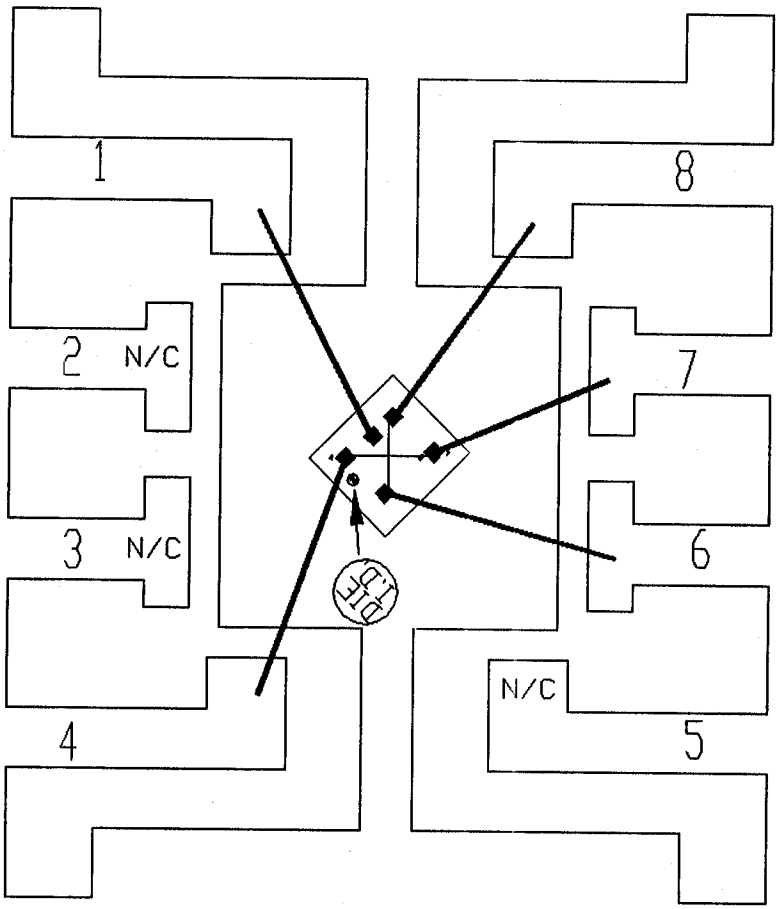


▨- BONDING AREA

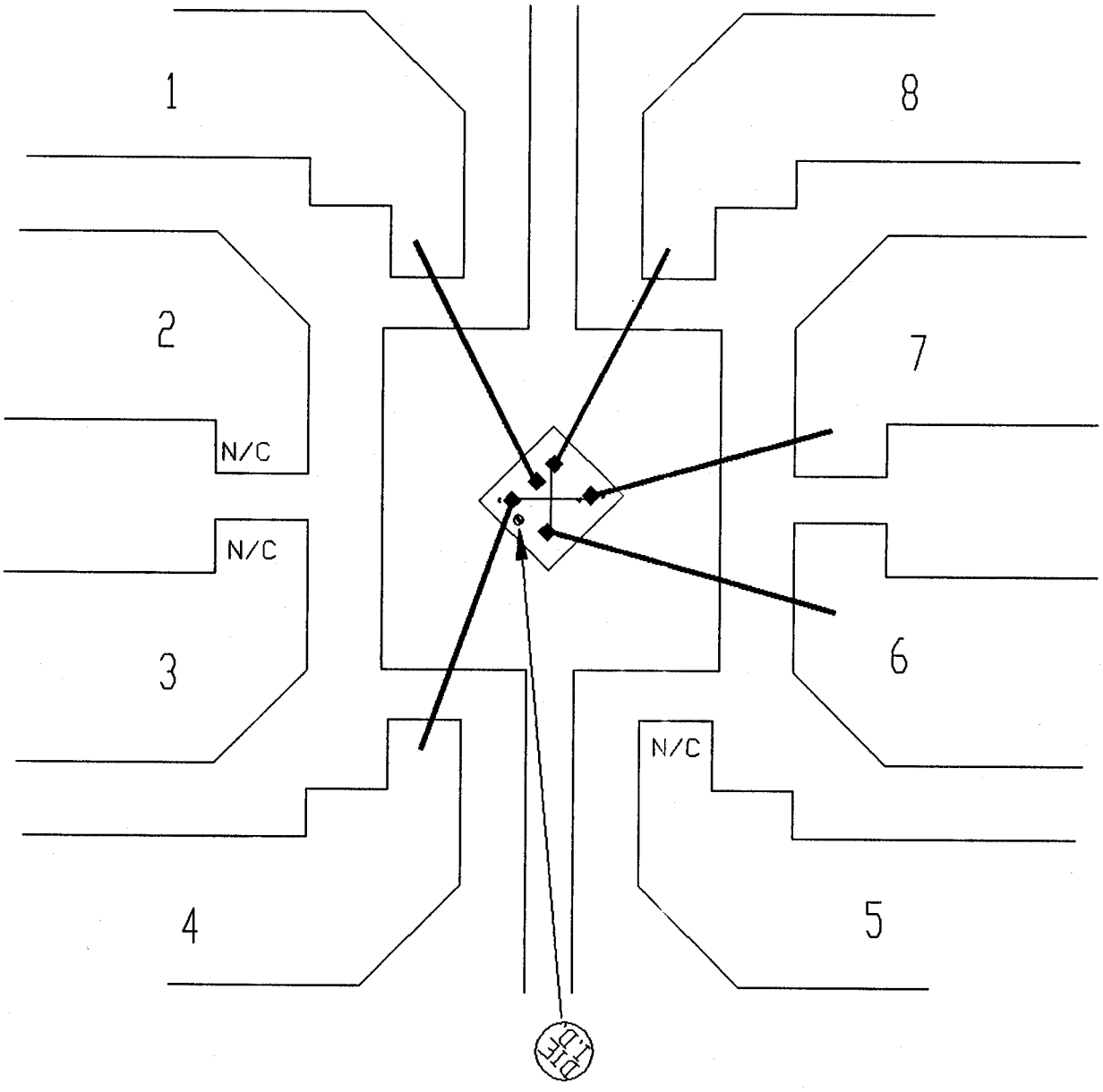
**USE NON-CONDUCTIVE EPOXY
DIE ATTACH 84-3J***

NOTE: CAVITY DOWN

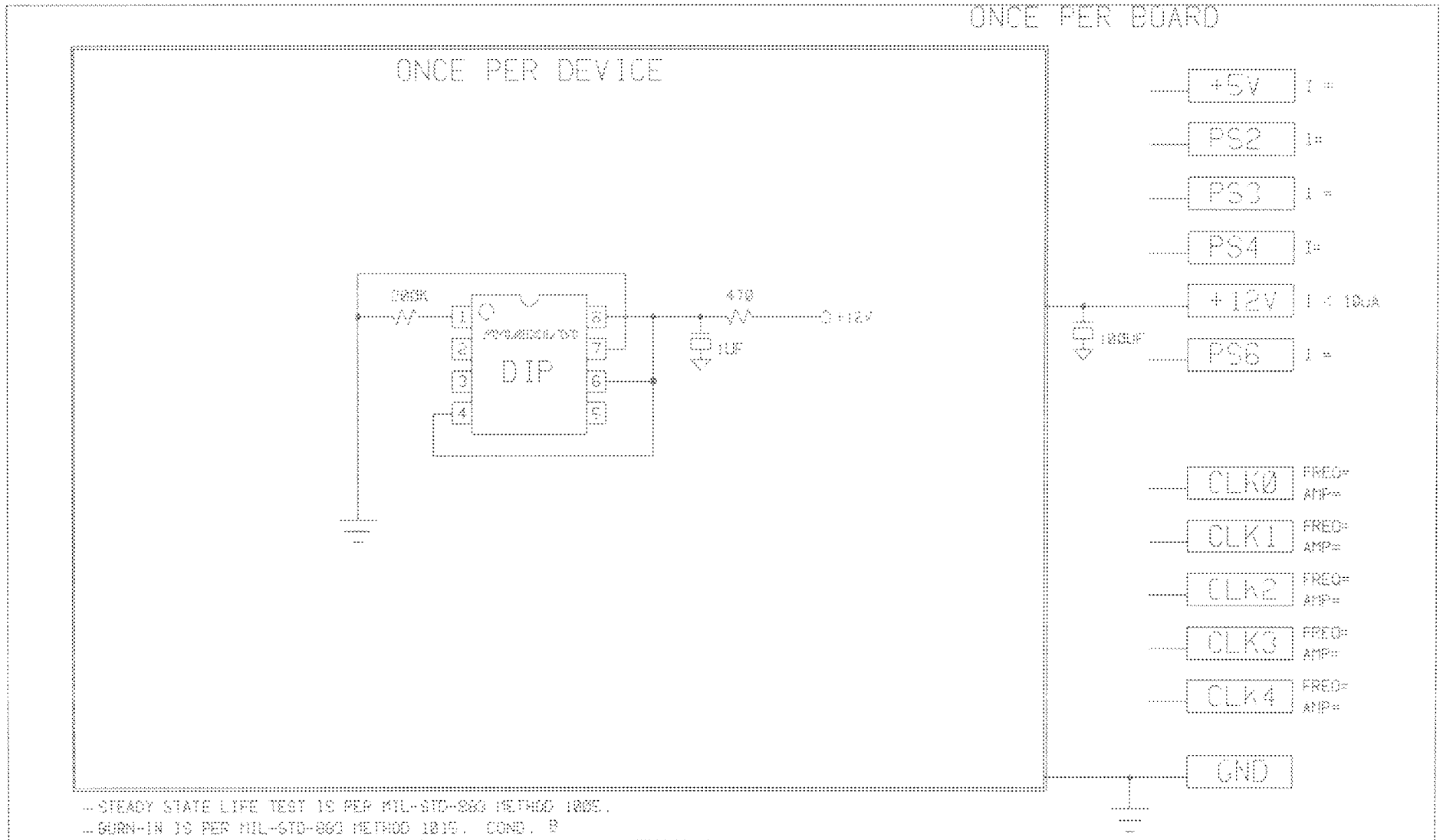
PKG.CODE: U5-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 64X45	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0766 / REV.: A



PKG.CODE: S8-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 90 X 90	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0765 / REV.: A



PKG.CODE: P8-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 100 X 100	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0764 / REV.: A



—STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
—BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] HR/883

SPEC. NO. 06-5174 REV: C

DATE: 4/19/96

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX4502/04/15/17