

RELIABILITY REPORT
FOR
MAX44264EWT+T
WAFER LEVEL PRODUCTS

April 30, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

| Approved by | | | |
|----------------------------------|--|--|--|
| Richard Aburano | | | |
| Quality Assurance | | | |
| Manager, Reliability Engineering | | | |



Conclusion

The MAX44264EWT+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

| IDevice Description | VQuality Assurance Information |
|-----------------------------|--------------------------------|
| IIManufacturing Information | VIReliability Evaluation |
| IIIPackaging Information | IVDie Information |
| Attachments | |

I. Device Description

A. General

The MAX44264 is an ultra-small (6-bump WLP) op amp that draws only 750nA of supply current. It operates from a single +1.8V to +5.5V supply and features ground-sensing inputs and rail-to-rail output. The ultra-low supply current, low-operating voltage, and rail-to-rail output capabilities make these operational amplifiers ideal for use in single lithium ion (Li+), or two-cell NiCd or alkaline battery systems. The rail-to-rail output stage of the MAX44264 is capable of driving the output voltage to within 4mV of the rail with a 100k load, and can sink and source 11mA with a +5V supply. The IC is unity-gain stable and available in a space-saving 0.9mm x 1.3mm, 6-bump WLP package.



II. Manufacturing Information

A. Description/Function: Ultra-Low Power Op Amp in a Tiny 6-Bump WLP

B. Process:B8C. Number of Device Transistors:D. Fabrication Location:USA

E. Assembly Location: Japan and USAF. Date of Initial Production: December 21, 2010

III. Packaging Information

A. Package Type: 6-bump WLP 3x2 array

B. Lead Frame: N/AC. Lead Finish: N/AD. Die Attach: None

E. Bondwire: N/A (N/A mil dia.)

F. Mold Material: None

G. Assembly Diagram: #05-9000-4163
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per Level 1

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: °C/W
K. Single Layer Theta Jc: °C/W
L. Multi Layer Theta Ja: 95°C/W
M. Multi Layer Theta Jc: °C/W

IV. Die Information

A. Dimensions: 37 X 53 mils

B. Passivation: Si3N4/SiO2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu
D. Backside Metallization: None

E. Minimum Metal Width: Metal1 = 0.8 / Metal2 = 1.2 microns (as drawn)

F. Minimum Metal Spacing: Metal1-2 = 1.2 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO₂I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = 1 \over MTTF = 1.83 \over 192 \times 4340 \times 48 \times 2$$
 (Chi square value for MTTF upper limit) (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

 $\lambda = 22.9 \text{ F.I.T. (60% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.02 @ 25C and 0.29 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot JM3ZAQ001A, D/C 1021)

The OY65 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.



Table 1Reliability Evaluation Test Results

MAX44264EWT+T

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|----------------------|--|----------------------------------|-------------|-----------------------|----------------------|
| Static Life Test (No | ote 1) Ta = 135C Biased Time = 192 hrs. | DC Parameters & functionality | 48 | 0 | JM3ZAQ001A, D/C 1021 |

Note 1: Life Test Data may represent plastic DIP qualification lots.