

RELIABILITY REPORT
FOR
MAX44263AXA+T
PLASTIC ENCAPSULATED DEVICES

July 31, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX44263AXA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX44260/MAX44261/MAX44263 offer a unique combination of high speed, precision, low noise, and low-voltage operation making them ideally suited for a large number of signal processing functions such as filtering and amplification of signals in portable and industrial equipment. The amplifiers feature an input offset of less than 50 μ V and a high-gain bandwidth product of 15MHz while maintaining a low 1.8V supply rail. The devices' rail-to-rail input/outputs and low noise guarantee maximum dynamic range in demanding applications such as 12- to 14-bit SAR ADC drivers. Unlike traditional rail-to-rail input structures, input crossover distortion is absent due to an optimized input stage with an ultra-quiet charge pump. The MAX44260 includes a fast-power-on shutdown mode for further power savings. The MAX44261 offers a unique on-demand calibration pin where the user can invoke self-trimming of the input offset voltage. The MAX44263 is a dual amplifier. The family of parts operates from a supply range of 1.8V to 5.5V over the -40°C to +125°C temperature range and can operate down to 1.7V over the 0°C to +70°C temperature range. The MAX44260/MAX44261 are available in small, 6-pin SC70 packages. The MAX44260 is also available in a 1mm x 1.5mm thin μ DFN (ultra-thin LGA) package. The MAX44263 is available in a small 8-pin SC70 package.

II. Manufacturing Information

A. Description/Function:	1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps
B. Process:	S18
C. Number of Device Transistors:	4482
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	September 28, 2012

III. Packaging Information

A. Package Type:	8-pin SC70
B. Lead Frame:	Copper
C. Lead Finish:	NiPdAu
D. Die Attach:	Non-conductive
E. Bondwire:	Au (.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5007
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	326°C/W
K. Single Layer Theta Jc:	115°C/W
L. Multi Layer Theta Ja:	326°C/W
M. Multi Layer Theta Jc:	115°C/W

IV. Die Information

A. Dimensions:	32.6772 X 40.9449 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO ₂
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

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| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAFC4Q001B, D/C 1219)

The OY69-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results
MAX44263AXA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	48	0	SAFC4Q001B, D/C 1219
	Biased	& functionality	32	0	SAFC4Q001C, D/C 1219
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.