RELIABILITY REPORT FOR

MAX44245ASD+T / MAX44245AUD+T

PLASTIC ENCAPSULATED DEVICES

October 26, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX44245ASD+T / MAX44245AUD+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX44244/MAX44245/MAX44248 family of parts provide ultra-precision, low-noise, zero-drift single/quad/ dual operational amplifiers featuring very low-power operation with a wide supply range. The devices incorporate a patented auto-zero circuit that constantly measures and compensates the input offset to eliminate drift over time and temperature as well as the effect of 1/f noise. These devices also feature integrated EMI filters to reduce high-frequency signal demodulation on the output. The op amps operate from either a single 2.7V to 36V supply or dual ±1.35V to ±18V supply. The devices are unity-gain stable with a 1MHz gain-bandwidth product and a low 90µA supply current per amplifier. The low offset and noise specifications and high supply range make the devices ideal for sensor interfaces and transmitters. The devices are available in µMAX, SO, SOT23, and TSSOP packages and are specified over the -40°C to +125°C automotive operating temperature range.

II. Manufacturing Information

A. Description/Function:	36V, Precision, Low-Power, 90µA, Single/Quad/Dual Op Amps	
B. Process:	S18	
C. Number of Device Transistors:	6838	
D. Fabrication Location:	USA	
E. Assembly Location:	Philippines, Thailand	Malaysia, Philippines, Thailand
F. Date of Initial Production:	June 27, 2013	

III. Packaging Information

A. Package Type:	14-pin SOIC (N)	14pin TSSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (0.8 mil dia.)	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#31-4914	31-4913
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	120°C/W	110°C/W
K. Single Layer Theta Jc:	37°C/W	30°C/W
L. Multi Layer Theta Ja:	82°C/W	100.4°C/W
M. Multi Layer Theta Jc:	32°C/W	30°C/W

IV. Die Information

A. Dimensions:	42.5197 X 105.5118 mils
B. Passivation:	Si3N4/SiO2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05@ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The OY90-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

With the following exceptions:
OUTD pin passes +100mA/-90mA per JEDEC JESD78

Table 1

Reliability Evaluation Test Results

MAX44245ASD+T / MAX44245AUD+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.