RELIABILITY REPORT

FOR

MAX4410EUD

PLASTIC ENCAPSULATED DEVICES

July 29, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

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Conclusion

The MAX4410 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4410 stereo headphone driver is designed for portable equipment where board space is at a premium. The MAX4410 uses a unique, patented, DirectDrive architecture to produce a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, board space, and component height.

The MAX4410 delivers up to 80mW per channel into a 16Ω load and has low 0.005% THD + N. A high power-supply rejection ratio (90dB at 1kHz) allows this device to operate from noisy digital supplies without an additional linear regulator, and includes ±8kV ESD protection. Comprehensive click-and-pop circuitry suppresses audible clicks and pops on startup and shutdown. Independent left/right, low-power shutdown controls make it possible to optimize power savings in mixed mode, mono/stereo applications.

The MAX4410 operates from a single 1.8V to 3.6V supply, consumes only 7mA of supply current, has short-circuit and thermal overload protection, and is specified over the extended -40°C to +85°C temperature range. The MAX4410 is available in a tiny (2mm x 2mm), 16-bump ultra chip-scale package (UCSP™) and a 14-pin TSSOP package.

B. Absolute Maximum Ratings

Item	Rating
PGND to SGND	-0.3V to +0.3V
PVDD to SVDD	-0.3V to +0.3V
PVSS to SVSS	-0.3V to +0.3V
PVDD and SVDD to PGND or SGND	-0.3V to +4V
PVSS and SVSS to PGND or SGND	-4V to +0.3V
IN_ to SGND	-0.3V to +0.3V
SHDN_to SGND	(SGND - 0.3V) to (SVDD + 0.3V)
OUT_ to SGND	(SVSS - 0.3V) to (SVDD +0.3V)
C1P to PGND	(PGND - 0.3V) to (PVDD + 0.3V)
C1N to PGND	(PVSS - 0.3V) to (PGND + 0.3V)
Output Short Circuit to GND or VDD	Continuous
Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
14 Lead TSSOP	727mW
Derates above +70°C	
14 Lead TSSOP	9.1mW/°C

II. Manufacturing Information

A. Description/Function:	80mW, DirectDrive Stereo Headphone Driver with Shutdown
B. Process:	S8 - Standard .8 micron silicon gate CMOS
C. Number of Device Transistors:	4337
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines or Thailand
F. Date of Initial Production:	April, 2002

III. Packaging Information

A. Package Type:	**14-Lead TSSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0121
H. Flammability Rating:	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions:	70 x 92 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 24.13 \times 10^{-9}$ $\lambda = 24.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5969) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AU08 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4410EUD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality (generic test vehicle)	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

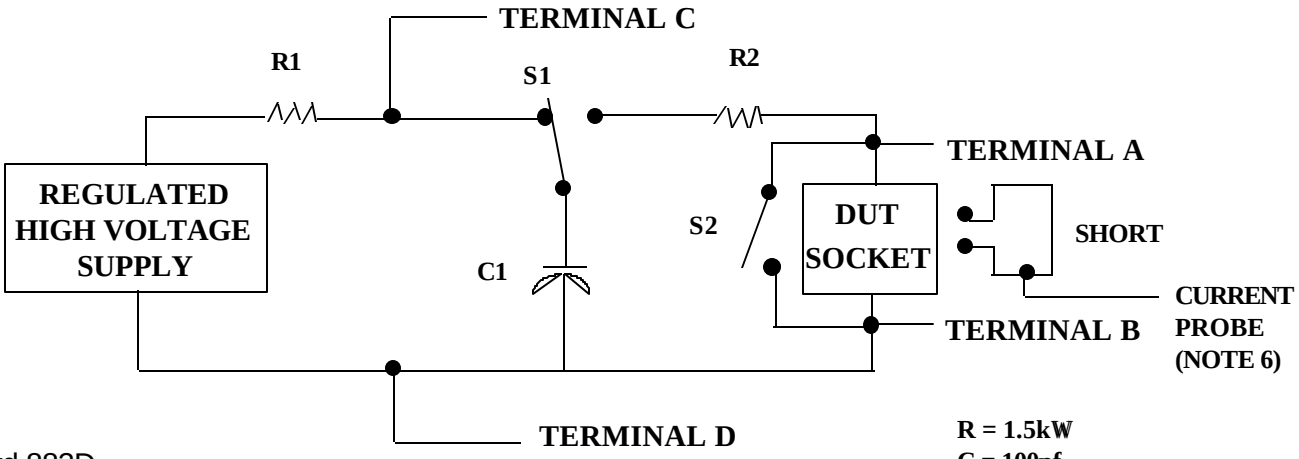
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

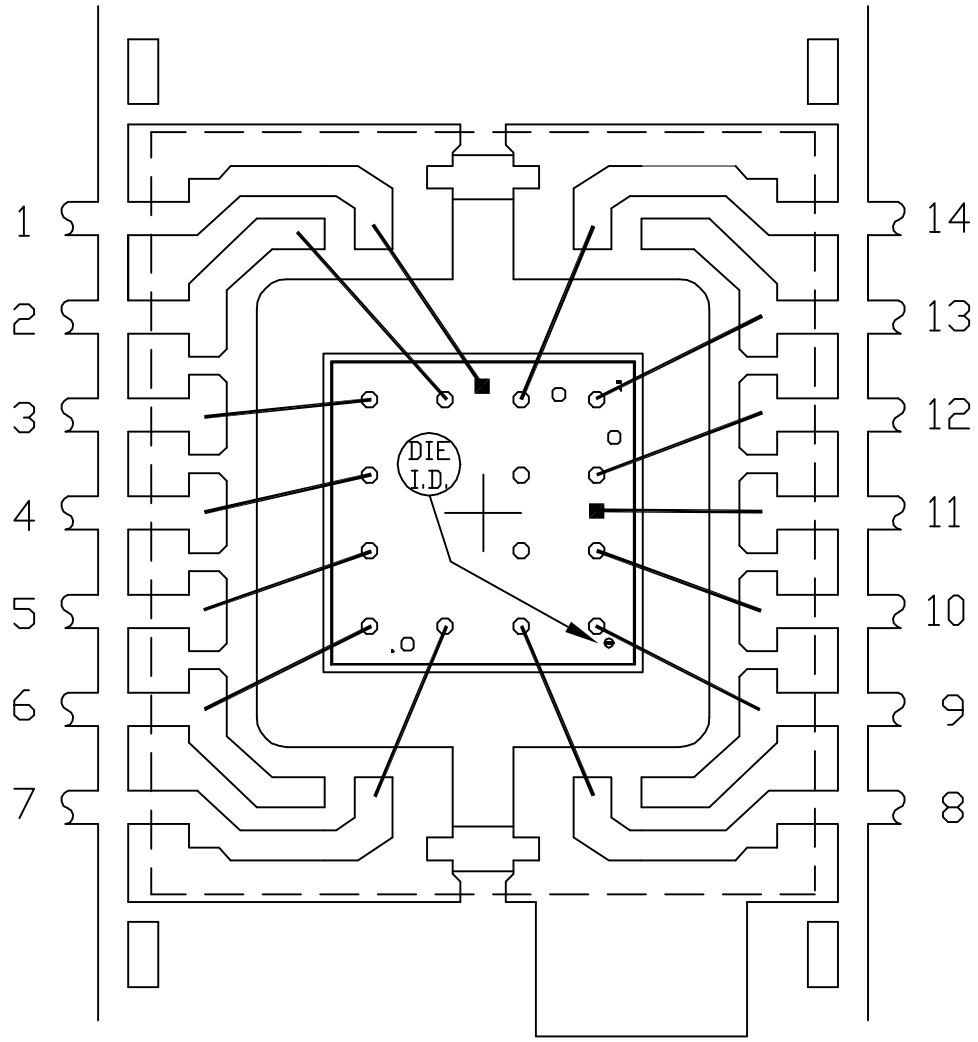
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



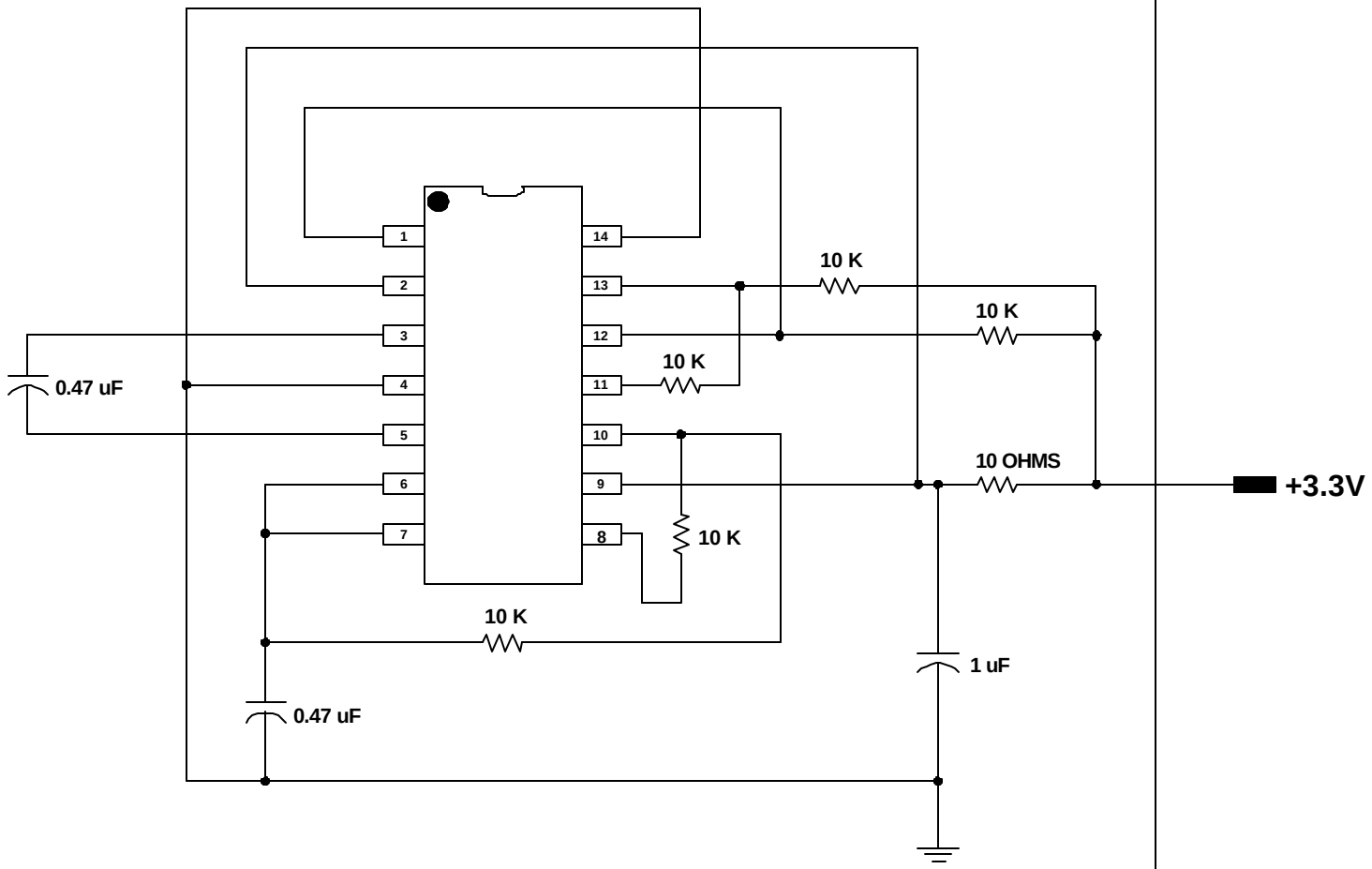
Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: U14-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118×122	PKG.			BOND DIAGRAM #: 05-9000-0121	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX4410
PACKAGE: 14-TSSOP
MAX. EXPECTED CURRENT = 11.5 mA

DRAWN BY: TEK TAN
NOTES: