MAX4390Exx Rev. A

RELIABILITY REPORT

FOR

MAX4390Exx

PLASTIC ENCAPSULATED DEVICES

January 13, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

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Conclusion

The MAX4390 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4390 op amp is a unity-gain stable devics that combine high-speed performance, Rail-to-Rail® outputs, and disable mode. This device is targeted for applications where an input or an output is exposed to the outside world, such as video and communications.

TheMAX4390 operates from a single 4.5V to 11V supply or from dual $\pm 2.25V$ to $\pm 5.5V$ supplies. The common-mode input voltage range extends to the negative power-supply rail (ground in single-supply applications). The MAX4390 consumes only 5.5mA of quiescent supply current per amplifier while achieving a 145MHz -3dB bandwidth, 35MHz 0.1dB gain flatness, and a 200V/µs slew rate. Disable mode sets the outputs to high impedance while consuming only 450µA of current.

Dating

The MAX4390 is available in a ultra-small, 6-pin SC70 package.

B. Absolute Maximum Ratings

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Rating
-0.3V to +12V (VEE - 0.3V) to (VCC + 0.3V) ±2.5V ±20mA Continuous -40°C to +85°C +150°C
-65°C to +150°C
+300°C
571mW
245mW
7.1mW/°C 3.1mW/°C

Note 1: Continuous power dissipation must also be observed.

II. Manufacturing Information

- A. Description/Function: Ultra-Small, Low-Cost, 145MHz Op Amp with Rail-to-Rail Outputs and Disable
- B. Process: CB20 (High Speed Complementary Bipolar Process)
 C. Number of Device Transistors: 396
 D. Fabrication Location: Oregon, USA
 E. Assembly Location: Malaysia
 F. Date of Initial Production: January, 2002

III. Packaging Information

A. Package Type:	5 Lead SOT-23	6 Lead SC70
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Non-Conductive Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-4301-0014	Buildsheet # 05-4301-0012
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	32 x 31 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Gold
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	2.7 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Jim Pedicord	(Reliability Lab Manager)
	Bryan Preeshl	(Executive Director)
	Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.

- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{\frac{1.83}{192 \times 4389 \times 80 \times 2}}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}$

λ = 13.57 x 10⁻⁹

 λ = 13.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5655) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The VA01 die type has been found to have all pins able to withstand a transient pulse of \pm 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of \pm 250mA.

Table 1Reliability Evaluation Test Results

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testin	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70 SOT23	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package. Note 2: Generic package/process data

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Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

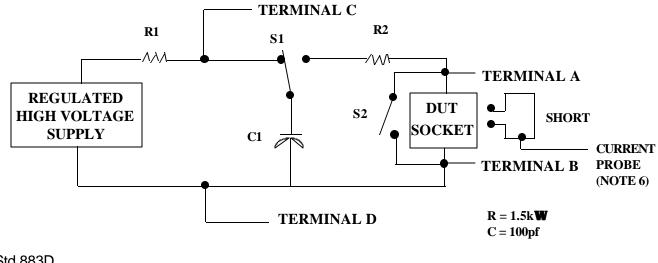
TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\frac{1}{2}$ No connects are not to be tested.
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

- 3.4 <u>Pin combinations to be tested.</u>
 - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
 - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

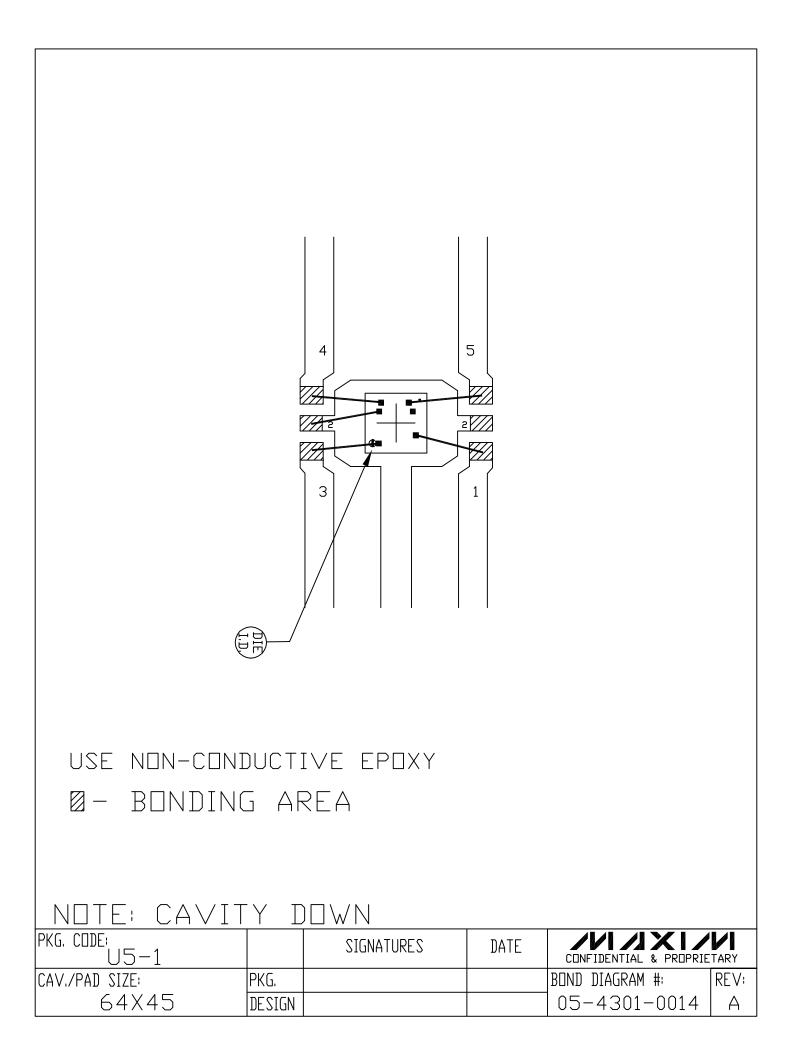
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

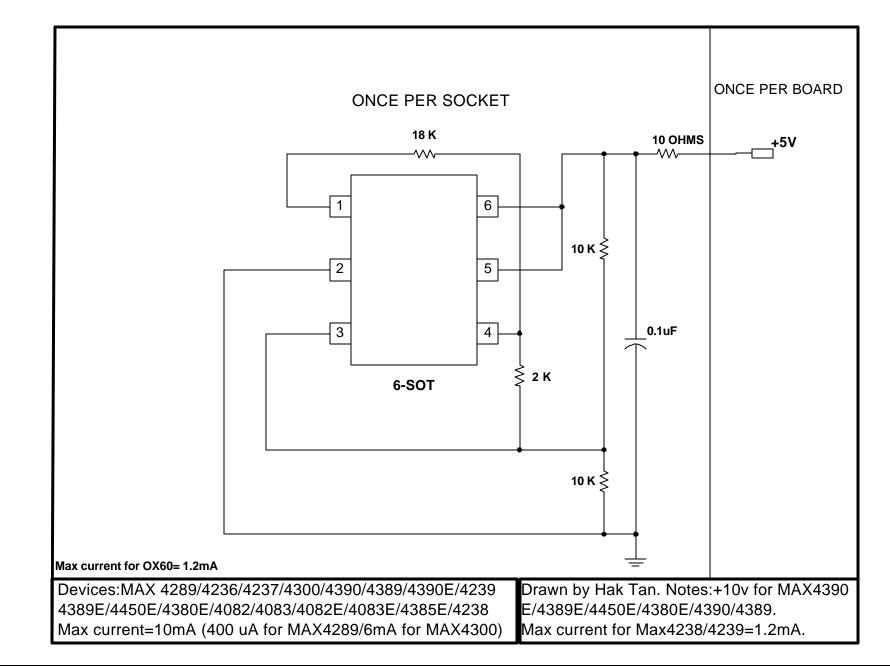


Mil Std 883D Method 3015.7 Notice 8

N/C 1/ USE NON-CONDUCTIVE EPOXY NDTE: CAVITY DOWN BONDABLE AREA

PKG. CODE: X6S-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
36×34	DESIGN			05-4301-0012	A





DOCUMENT I.D. 06-5655	REVISION E	MAXIM TITLE: BI Circuit	PAGE 2 OF 3
		(MAX4289/4236/4237/4300/4390/4389/4390E/4389E/4450E/4380E/4082/4083/4082E/4	
		083E/4385E/4238/4239)	