MAX4382Exx Rev. A

**RELIABILITY REPORT** 

FOR

# MAX4382Exx

PLASTIC ENCAPSULATED DEVICES

January 29, 2003

# **MAXIM INTEGRATED PRODUCTS**

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#### Conclusion

The MAX4382 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. .....Device Description II. .....Manufacturing Information III. .....Packaging Information IV. .....Die Information V. .....Quality Assurance Information VI. .....Reliability Evaluation

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#### I. Device Description

A. General

The MAX4382 op amp is a unity-gain-stable device that combine shigh-speed performance, Rail-to-Rail<sup>®</sup> outputs, and high-impedance disable mode. This device operates from a +4.5V to +11V single supply or from  $\pm 2.25V$  to  $\pm 5.5V$  dual supplies. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications).

The MAX4382 requires only 5.5mA of quiescent supply current per op amp while achieving a 210MHz -3dB bandwidth, 55MHz 0.1dB gain flatness and a 485V/µs slew rate. This device is an excellent solution in low-power/low-voltage systems that require wide bandwidth, such as video, communications, and instrumentation.

#### B. Absolute Maximum Ratings

12V /EE - 0.3V) to (VCC + 0.3V) s
10°C to +85°C 150°C 5°C to +150°C 300°C
27mW 67mW 67mW 1mW/°C .3mW/°C .3mW/°C

## II. Manufacturing Information

A. Description/Function: Ultra-Small, 210MHz, Single-Supply Op Amp with Rail-to-Rail Outputs and Disable

B. Process:	CB20 (High Speed Complementary Bipolar Process)
C. Number of Device Transistors:	196
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines, Korea or Thailand
F. Date of Initial Production:	April, 2001

#### **III.** Packaging Information

A. Package Type:	14-Lead TSSOP	14-Lead SO	16-Lead QSOP
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-2501-0111	# 05-2501-0112	# 05-2501-0113
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

#### **IV. Die Information**

A. Dimensions:	52 x 60 mils
B. Passivation:	$Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Gold
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	2.7 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

#### V. Quality Assurance Information

A. Quality Assurance Contacts:	Jim Pedicord	(Reliability Lab Mana
	Bryan Preeshl	(Executive Director)
	Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.

- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

#### **VI.** Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

Manager)

 $\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 80 \times 2}$  (Chi square value for MTTF upper limit) Temperature Acceleration factor assuming an activation energy of 0.8eV

 $\lambda = 29.97 \times 10^{-9}$ 

 $\lambda = 29.97$  F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In. Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5288) shows the static Burn-In circuit. Maxim also performs guarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

#### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

#### C. E.S.D. and Latch-Up Testing

The OX73 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

# Table 1Reliability Evaluation Test Results

TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
(Note 1)				
Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	1
ng (Note 2)				
Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP SO QSOP	77 77 77	0 0 0
Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
ess (Note 2)				
-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0
	(Note 1) $Ta = 135^{\circ}C$ Biased Time = 192 hrs. Tg (Note 2) $Ta = 121^{\circ}C$ P = 15  psi. RH= 100% Time = 168hrs. $Ta = 85^{\circ}C$ RH = 85% Biased Time = 1000hrs. ess (Note 2) $-65^{\circ}C/150^{\circ}C$ 1000  Cycles	IDENTIFICATION(Note 1) Ta = 135°C Biased Time = 192 hrs.DC Parameters & functionality Time = 192 hrs.ng (Note 2)Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.DC Parameters & functionality RH= 100% Time = 168hrs.Ta = 85°C RH = 85% Biased Time = 1000hrs.DC Parameters & functionalityess (Note 2)-65°C/150°C 1000 CyclesDC Parameters DC Parameters	IDENTIFICATIONPACKAGE $(Note 1)$ Ta = 135°C Biased Time = 192 hrs.DC Parameters & functionality Time = 192 hrs.ng (Note 2)Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.DC Parameters & functionality SO QSOPTa = 85°C RH = 85% Biased Time = 1000hrs.DC Parameters & functionalityess (Note 2)-65°C/150°C 1000 CyclesDC Parameters DC Parameters & functionality	IDENTIFICATIONPACKAGESIZE(Note 1) Ta = 135°C Biased Time = 192 hrs.DC Parameters & functionality Time = 192 hrs.80rg (Note 2)Ta = 121°C P = 15 psi. 

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Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package. Note 2: Generic package/process data

### Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V <sub>PS1</sub> <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

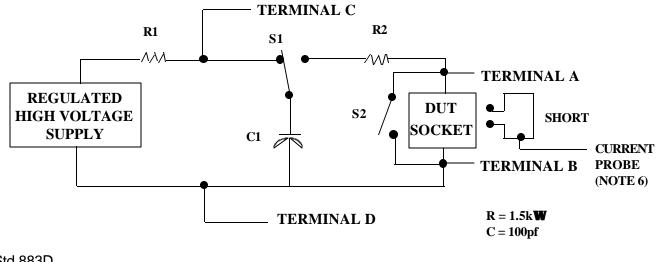
TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2}$  No connects are not to be tested.
- $\overline{3'}$  Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_{S}$ ,  $-V_{S}$ ,  $V_{REF}$ , etc).

- 3.4 Pin combinations to be tested.
  - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
  - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V<sub>SS1</sub>, or V<sub>SS2</sub> or V<sub>SS3</sub> or V<sub>CC1</sub>, or V<sub>CC2</sub>) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8

