

RELIABILITY REPORT

FOR

MAX4350EUK+

PLASTIC ENCAPSULATED DEVICES

September 8, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX4350EUK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4350 single and MAX4351 dual op amps are unity-gain-stable devices that combine high-speed performance with rail-to-rail outputs. Both devices operate from dual ±5V supplies. The common-mode input voltage range extends to the negative power-supply rail. The MAX4350/MAX4351 require only 6.9mA of quiescent supply current per op amp while achieving a 210MHz -3dB bandwidth and a 485V/µs slew rate. Both devices are excellent solutions in low-power systems that require wide bandwidth, such as video, communications, and instrumentation. The MAX4350 is available in an ultra-small 5-pin SC70 package and the MAX4351 is available in a space-saving 8-pin SOT23 package.



II. Manufacturing Information

A. Description/Function: Ultra-Small, Low-Cost, 210MHz, Dual-Supply Op Amps with Rail-to-Rail

Outputs CB20

B. Process:

C. Number of Device Transistors:

D. Fabrication Location: Oregon
E. Assembly Location: Malaysia
F. Date of Initial Production: July 24, 1999

III. Packaging Information

A. Package Type: 5L SC70
B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)

F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-2501-0002 / B
H. Flammability Rating: Class UL94-V0

Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: 324°C/W
K. Single Layer Theta Jc: 115°C/W
L. Multi Layer Theta Ja: 324°C/W
M. Multi Layer Theta Jc: 115°C/W

IV. Die Information

A. Dimensions: 31 X 31 mils

B. Passivation: Si₃N₄ (Silicon nitride)

C. Interconnect: Au

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO₂I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm
D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (3) is calculated as follows:

$$_{\lambda}$$
 = $\frac{1}{\text{MTTF}}$ = $\frac{1.83}{192 \times 4340 \times 80 \times 2}$ (Chi square value for MTTF upper limit)

 $_{\lambda}$ = 13.7 x 10⁻⁹
 $_{\lambda}$ = 13.7 x 10⁻⁹
 $_{\lambda}$ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the CB20 Process results in a FIT Rate of 0.14 @ 25C and 2.48 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot N7VAAQ001B, D/C 9917)

The OX13 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-100mA.



Table 1Reliability Evaluation Test Results

MAX4350EUK+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (No	ote 1) Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	N7VAAQ001F, D/C 9926

Note 1: Life Test Data may represent plastic DIP qualification lots.